Research Journal of Recent Sciences _____ ISSN 2277-2502
Vol. **7(7),** 31-34, July **(2018)** *Res. J. Recent Sci.*

Short Review Paper

Design of complementary metal oxide semiconductor inverter

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Available online at: www.isca.in, www.isca.me
Received 15th November 2017, revised 26th May 2018, accepted 24th June 2018

Abstract

Power MOSFET IRF9140 and IRF150 from OrCAD library were used to design the CMOS inverter. Keeping their size in the ratio of 2:1 the design and evaluations are carried out through simulation in OrCAD capture environment. The inverter circuit is optimized to yield the optimal noise margin and time delay response. The evaluation presents the analysis of voltage transfer characteristics and its transient response. Through the evaluation of voltage transfer characteristics, high noise margin of 4.80V and low noise margin of 4.56V is achieved. The evaluated maximum power dissipation is 48W. The evaluation of transient response resulted into the rise and fall time delay of 0.057µS and 0.048µS. The paper presents the detailed evaluation of power MOSFET based CMOS inverter.

Keywords: Complementary metal oxide semiconductor (CMOS), voltage transfer characteristics, noise margin.

Introduction

Complementary metal oxide semiconductor, also known as CMOS technology. It plays a major role inchip design in the computer industry and mostly used to build integrated chips[1]. It's application also can be found under several analog circuits including image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. CMOS is the building blocks for most of the Very Large Scale Integration (VLSI) digital circuits[2]. The important characteristics of CMOS devices are; low static power consumption, relatively high speed, high noise margin in both state and ease of implementation in the transistor level[3]. Substantial power draws only when transistors are at the switching state which results in lower heat wastage in CMOS devices unlike NMOS technology, which have standing current even when it is not in its changing state[4].

One of the most essential component of CMOS technology is the CMOS inverter. Inverters are the most basic logic which are able to perform a Boolean operation just with a single input[5]. PMOS acts as pull-up network and NMOS acts as pull-down network. PMOS is connected to Vdd at its source while NMOS source is connected to ground as shown in Figure-1. The input is applied on gate-source terminal and output is taken from drain-source terminal. The evaluation of CMOS inverter is carried out using IRF150 and IRF9140 from EVAL library in OrCAD Capture environment. IRF150[6] is an N-Channel enhancement mode silicon gate power FET. Whereas IRF9140 is a 100V single P-Channel power MOSFET featuring efficient geometry and unique processing with very low on-state resistance combined with high transconductance[7]. IRF150 was used from EVAL library and IRF9140 from EVALAA library in the simulation environment of OrCAD Capture. The paper presents the characteristics evaluation of CMOS inverter using mentioned power MOSFET's. The evaluation includes the analysis carried out by finding its noise margin, transient response characteristics and the power consumed by the inverter.

Voltage Transfer Characteristics (VTC)

Figure-1 shows the basic CMOS inverter. Biasing voltage V2 of 10V is applied to the inverter. A RC parallel network is connected towards the output of the inverter with Resistor of 1kΩ and Capacitor of 0.1µF. To achieve the VTC[8] the gate dc voltage applied at the input of the inverter is linearly increased from zero. The corresponding VTC of the inverter is shown in Figure-2.

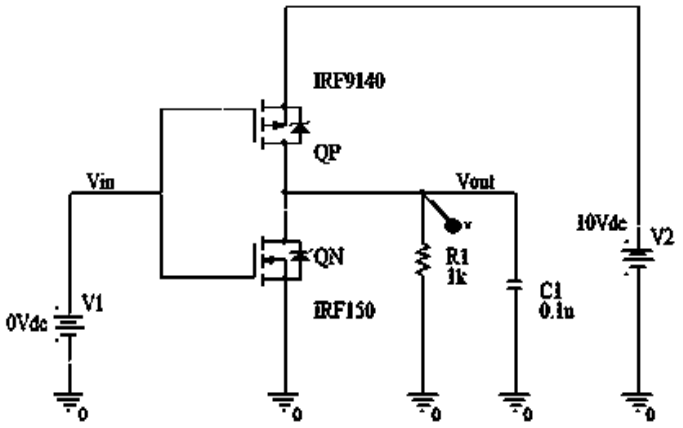

Figure-1: Circuit Diagram of CMOS inverter.

Table-1: Operating Region of CMOS Inverter.

Region	QN(NMOS)	QP(PMOS)
A	Cut-off	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cut-off

When zero volt is applied at the input of the inverter strong E-field in the gate region is built up forming a channel in the P-region. Under this condition the PMOS (QP) turns ON due to forward biasing. The MOSFET operates in the linear region. The NMOS (QN) device still remains in its off condition as the input voltage is lesser than its threshold ($Vi=V_{GS}<V_{TN}$).Where, V_{TN} and V_{TP} is the threshold voltage of NMOS and PMOS transistor. The power dissipation is zero. When the input voltage is increased, the output voltage remains same until the threshold voltage, V_T. When it reaches the threshold voltage, the PMOS operates in the linear region as it has sufficient forward bias and N- Channel starts conducting and switches instantly to saturation as it still has a comparatively adequate VDS across it. At this point, both the transistors are conducting. The PMOS transistor stays in the linear region ($V_{SD}<=V_{SG}+V_{TP}$) whereas the NMOS transistor in the saturation region ($Vi=V_{DS}>=V_{GS}-V_{TN}=Vo-V_{TN}$). Under this condition, the Power dissipation is no longer zero. In the middle of the VTC, a point or a region occurs where input voltage (Vi) is equal to the output voltage (Vo). It is labeled as V_E and is identified as the gate threshold voltage. At this point, an equal voltage is dropped across NMOS transistor and the PMOS transistor. Both the transistors operate in a saturation region for this instant of time as they have sufficient forward bias voltage. The power at this instant, touches to the peak, where $V_E=Vi=Vo$.

Now when the input voltage is slightly increased beyond VE but lower than $V_{DD}-V_{TP}$, the PMOS transistor moves to the saturation region ($V_{SD}>=V_{SG}+V_{TP}=V_{DD}-Vo+V_{TP}$).The NMOS transistor being in forward biased ($Vi=V_{GS}> V_{TN}$) turns on. The NMOS stays in linear region. When input voltage is further increased, N-channel conducts better and P-channel conducts less. Eventually, when the input voltage is at V_{DD}, the PMOS transistor falls on the cut-off and NMOS transistor operates in the linear region. The summarized operating regions along the VTC curve corresponding to individual MOSFET is given in Table-1.

To evaluate the noise margin[9] of the inverter the following voltage parameters were recorded. The recorded parameters are output low voltage (VOL), output high voltage (VOH), input low voltage (VIL) and input high voltage (VIH).

Where, VOL – 0V, VOH = 10V, VIL = 4.56V, VIH=5.185V. Therefore, the evaluated NMH (high noise margin) = VOH – VIH = 4.8V.

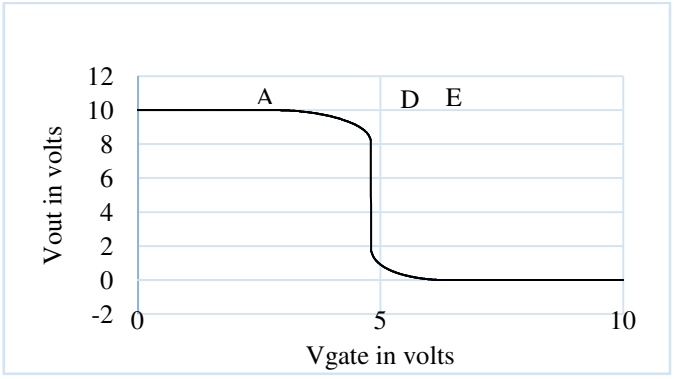

Figure-2: VTC of CMOS inverter.

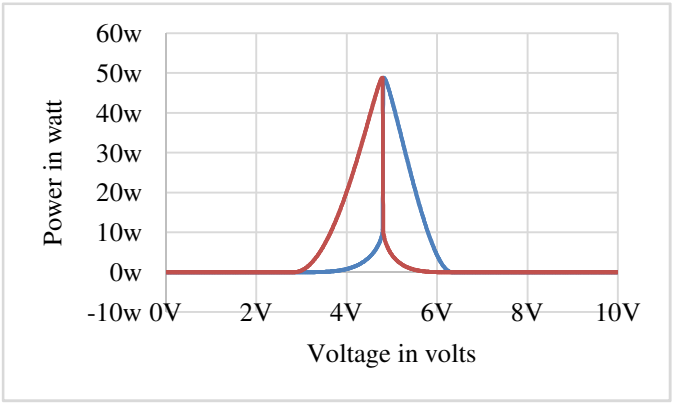

Figure-3: Power Consumption of Inverter.

The evaluated power dissipation of the CMOS inverter is given in Figure-3. From the figure, the maximum power dissipation occurs at VE, when both the transistors are operating at saturation region. The evaluated maximum consumed power is 48W as shown in the Figure-3. In the figure, the brown colored curve shows the power consumed by NMOS and the blue colored curve shows the power consumed by PMOS transistor. In a saturation region, the NMOS and PMOS transistors consume nearly equal power. Thus, CMOS is having virtually no static power dissipation in either the logic 1 or logic 0 state[10].

Transient response of CMOS Inverter

For the evaluation of inverter's transient response, a voltage pulse source is applied at the input of the inverter. The pulse with pulse width of 10µS was applied with duty cycle of 50%. Its rising and fall time were 1nS each with time delay of zero seconds. The adapted circuit is presented in Figure-4. Figure-5 presents its corresponding output.

In Figure-5 shows the output pulse of the inverter. Seen mildly from the figure, there exist a slight delay in the output pulse-giving rise to imperfect rise and fall time of the output. To

analyze the delay in fall time, the falling up pulse region is magnified as shown in Figure-6. From the figure, the time taken for the output signal to fall from 90% of the total output to its 10% of full voltage was evaluated as 0.0408µs. The detail evaluation is shown in Figure-6.

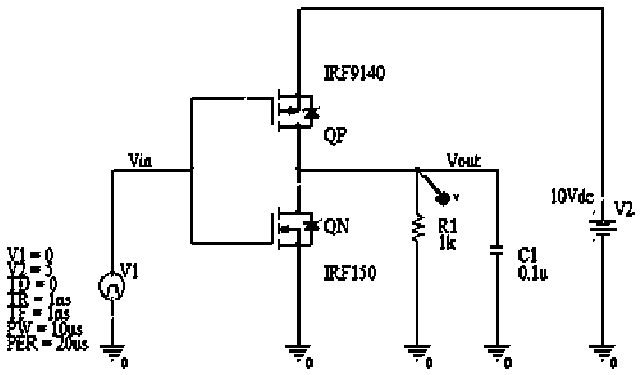

Figure-4: Circuit diagram of CMOS inverter.

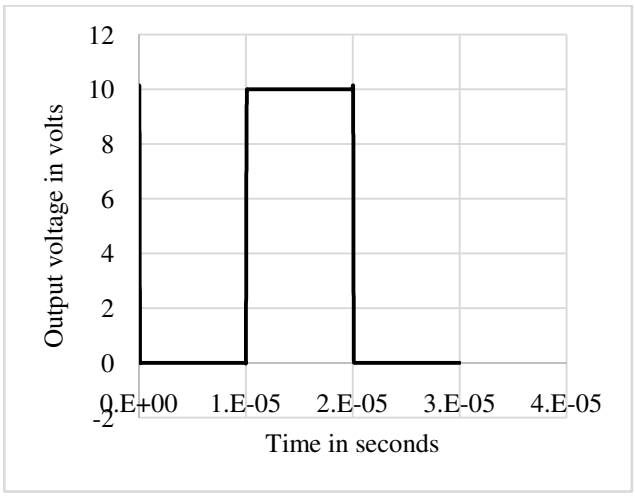

Figure-5: Transient response of CMOS.

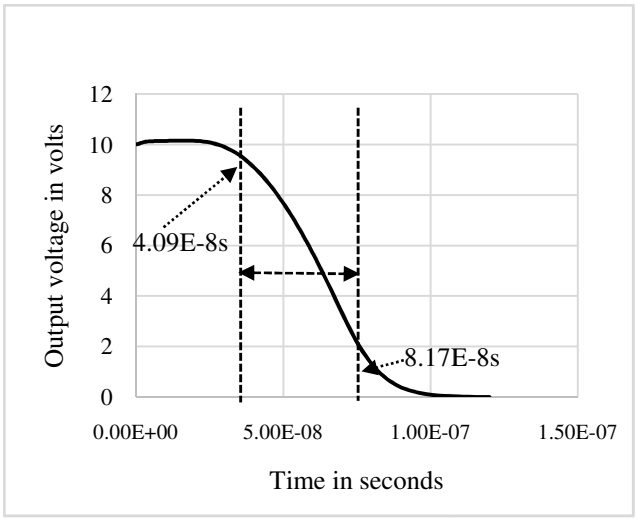

Figure-6: Fall time evaluation.

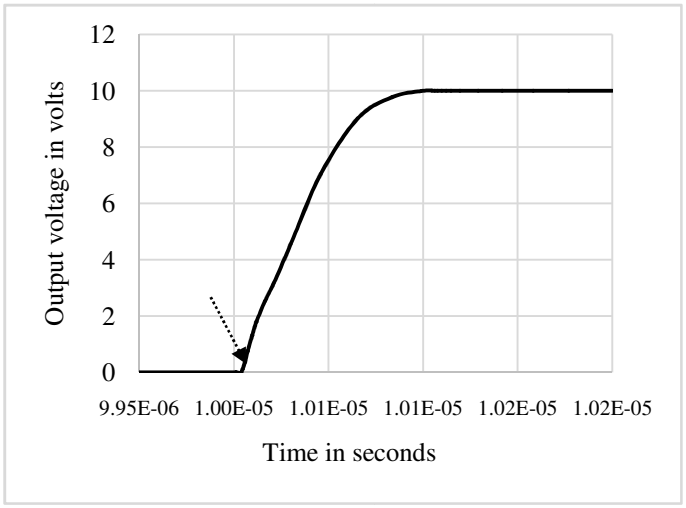

Figure-7: Rise time evaluation.

Similarly, the evaluation of rise time was carried out and its analysis is shown in figure 7. From the above figure, the time taken for the output signal to completely rise from 10% of the total output to 90% is 0.1µs

Conclusion

IRF library from OrCAD Capture were used to evaluate the characteristics of CMOS inverter. Two power MOSFET's, IRF9140 and IRF150 were used to design CMOS inverter. The evaluation of the CMOS inverter includes the design, simulation, and analysis of VTC and the transient response. In addition, the evaluation of power consumed by the inverter is also presented. To achieve the best result for its analysis the resistor, capacitor and the input frequency were optimized. The optimized values are resistor of 1kΩ, capacitor of 0.1uF and frequency of 50KHz respectively. These optimized parameters have resulted into good power MOSFET based CMOS inverter with rise time delay of 0.1µS and fall time delay of 0.0408µS. The high noise margin and low noise margin obtained were 4.8volts and 4.56 volts. The maximum power consumed by the designed inverter is 48W. The sizes of PMOS and NMOS was kept at a ratio of 2:1.

Acknowledgement

We wish to acknowledge and express our personal gratitude to all those without whom completion of this task would be impossible. Then ISC for providing us the platform to present our paper and enhance our research skills. We also would like to thank the college management and our friends for supporting and providing us with continuous supports.

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