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Design of HSDPA System with Turbo Iterative Equalization

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Abstract

High Speed Packet data Access (HSPA) has been designed to increase packet data performance, higher data service and lowest bit rates .HSDPA receiver was designed in terms of computation requirement and power consumption from the Turbo Decoder by effectively deploying pipelining or parallelism. The parallelism on the Architecture is proposed to achieve the high-throughput demand for turbo decoder for Fourth Generation (4G) wireless communication systems. The Multiple soft-in/soft-out (SISO) decoders are used to achieve parallel architecture. The soft-output decisions are performed through an iterative process and achieved by soft-input soft-output (SISO) multi-code detector and a SISO turbo decoder. The parallel architecture leads to conflicts during memory accesses. A complete memory conflict analysis for different interleaver patterns has been performed and shows the effect of using different decoding configurations on the memory conflicts for different standards. This can be reduced significantly from the conflict. The iteration is based on the priority information, first the detected information is extracted and Decoded then the priority information is used for the next iteration. From the result we can see the significance performance gain over the receiver structure from the turbo iterative structure with chip equalization.

Keywords: HSDPA, code detection, memory conflict, bit-rate, turbo decode process.

Introduction

In wireless communication systems, the HSDPA is an important standard for W-CDMA (Wideband Code Division Multiple Access) improving communications reliability. The turbo code is the most significant breakthrough in the field of channel coding from the introduction of trellis codes. HSDPA support multimedia services by employing high peak data rate transmission up to approximately 10Mbps and it is achieved by applying Turbo Decoding. In any communication system which requires high throughput, adequate area, and low power are achieved by Turbo decoding. By effectively designing Turbo decoder we can improve the overall system performance. In HSDPA system Multipath propagation is used to destroy the Orthogonality among the spread signals and it causes the MCI. The reliable CDMA communications in multipath are achieved in the presence of both MCI and inter symbol interference (ISI).

The future wireless devices which will be made from additional and higher specifications than the current standards involved also be compatible with the same platforms which exist in the markets. The general purpose processor (GPP) fulfills the complete flexibility at the expense of the power and the throughput requirements. Initially the throughput is very low because the instructions and the architectures are not designed for wireless system domains. In wireless devices low power consumption is an important goal should be achieved in. The digital signal processor (DSP) is also convenient for transferring from one standard to another. Turbo codes contain the source of memory conflicts. The interleaver patterns affect the memory conflicts. There are two types of interleaver are used in memory conflicts, unconstrained interleaver and constrained interleaver. The constrained interleaver are called maximum contention free (MCF) which mean no conflicts occur due to parallel accesses[1] in the transmitter.

In this paper we propose a novel turbo iterative receiver structure with chip equalization (TIRCE) to improve the performance of the HSDPA systems. The chip equalization is used to improve the accuracy of the system from the iterative decoding process, and multi-code detection and turbo decoding are tightly coupled to maximize the overall gain.

Prior Work

The Past few years HSDPA architecture design has so many proposals modification from the Parallel Turbo Decoder design and its effects on the memory conflicts have received much attention. The turbo code design[2] a unified parallel radix-4 Turbo decoder architecture design[3] is proposed to support WiMAX and 3GPP-LTE standards in order to achieve the maximum performance with high speed data rate. However these works are limited by the turbo standards and cannot support the remaining standards. The Memory mapping algorithm[4] was designed to avoid any contention by cascading three different layers of permutation. But the designed method does not optimize neither the cost of the architecture nor the throughput by calculating the latency from the execution. A

general-interleaved-Bottleneck-Breaker node (GIBB)[5] was designed based on a random graph generation algorithm by avoiding the conflicting access through building a network. But these nodes are not efficient due to its complex routing and resources. But the targeted memory conflict data was proposed[6] to avoid memory contentions, but the determined buffer size was not efficient in terms of RTL model. Similarly the design can support only one standard and not suitable for multi-standard configuration. The proposed buffer was designed[7] to analyze memory conflicts by reducing the area and higher operating frequency is achieved by adding variable delay department in the design by selecting standard case instead of worst case

An efficient memory conflict for multi-standards Turbo decoders[8] was provided for memory consideration. However, the memory conflicts for the unified parallel radix-4 Turbo decoder and some standards have not been analyzed. The analysis of memory conflicts for a unified parallel radix-4 Turbo decoder[9] was provided to avoid the memory mismatch . The bigger size FIFO sizes are used in HSDPA standard to avoid the contents on the memories in the iteration by adding extra cycles.

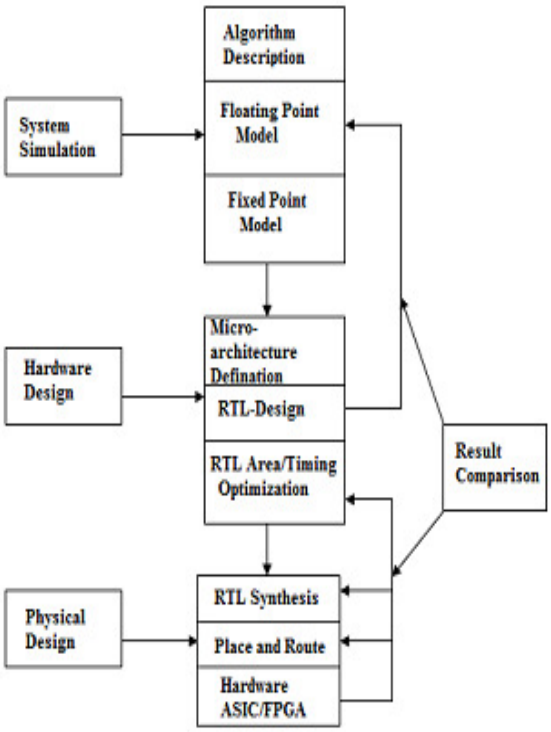

Figure-1
Design flow approach from the top level design to ASIC/FPGA design

Design Flow

The typical RTL design approach, as shown in Figure 1, consists of three main steps: System simulation to ensure correct functionality, which is done using high level languages like MATLAB, C., Hardware design to implement the system towards the ASIC, which is done using Hardware description languages like Verilog HDL, VHDL, Physical design to convert the obtained HDL into real chip.

The result comparisons are performed after each step to ensure the correctness of the design

Turbo Decoder Algorithms

The Turbo decoding process is an iterative process consisting of two Soft in Soft out (SISO) Maximum Aposterior Probability (MAP) decoders, as shown in figure-2. In communication channel the transmitted soft signal was received in the MAP decoder. The received extrinsic information is passed for the iteration by keeping the received signal constant and the iteration process will be done based on the extrinsic information, but decoding is done in many times. The LLR ratio is calculated in the decoder by intrinsic LLR from the communication channel and the extrinsic LLR added by the decoder itself. After the each iteration the extrinsic information is passed from the decoder for the next iteration and the decoder algorithm requires several iterations to calculate the transmitted data and the final destination is made from the two SISO decoder extrinsic information by demodulating the soft bits.

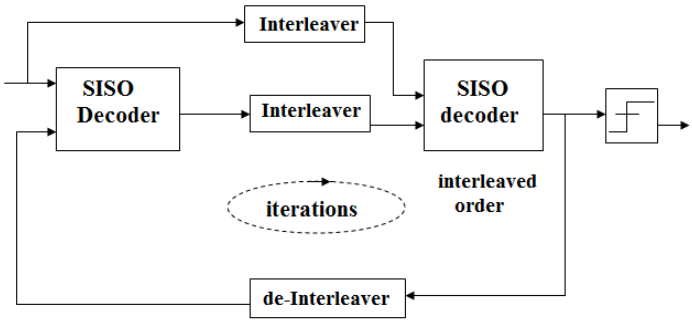

Figure-2
SISO decoder

In[1] the probability estimation of state transition is calculated from the BCJR algorithm. The modification in the algorithm is done based on the MAP (maximum a posteriori) algorithm. Due to its SISO property it is suitable for iterative turbo decoding. The main advantage of the soft output is used to get the accurate value by its iteration property. In this algorithm the calculation of numerical problems and unnecessary calculation can be avoided by log domain algorithm, after that this algorithm is called as log-MAP algorithm. All numerical problems and unnecessary multiplications are performed based on this algorithm to avoid the unnecessary multiplication and other mathematical problems. But using this method the designer requires the more amounts of hardware resources to implement this algorithm. Due to the above simplification algorithm there

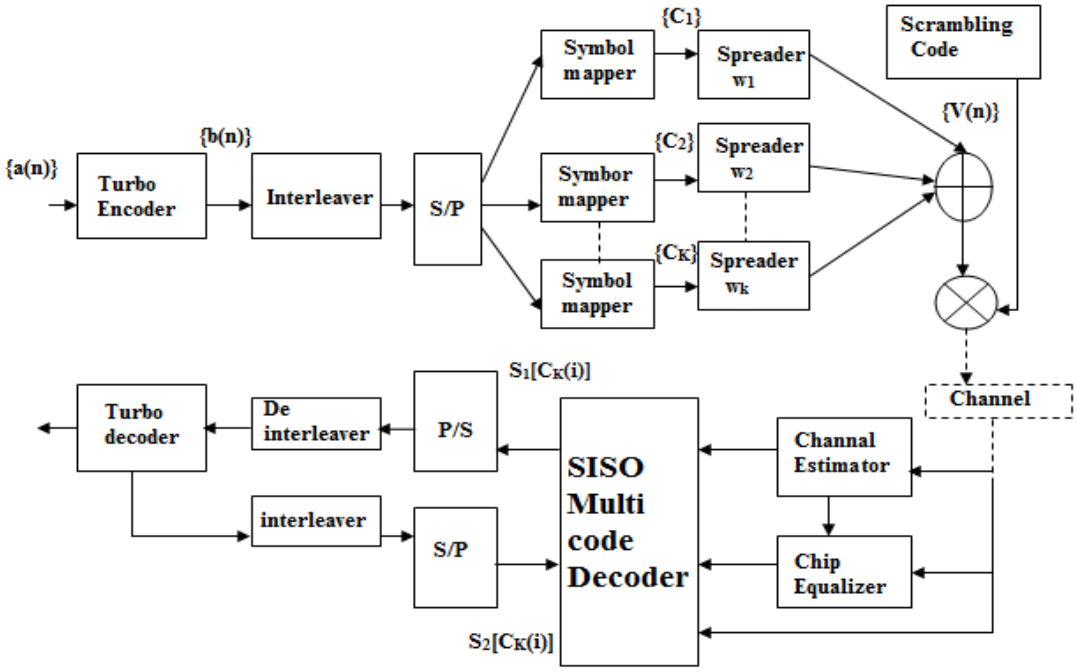

Figure-3
Turbo HSDPA receiver structure

may be a possibility in performance degradation while implementing the algorithm and it is recovered by linear-log-MAP and constant-log-MAP. and Max-log-MAP [11] and it is compensated by enhancement Max-Log-MAP where a scaling factor scales the extrinsic LLRs

HSDPA and Turbo Iterative Receiver Model

HSDPA model: As illustrated in figure-3 in the turbo decoding algorithm is the iteration between two soft-input soft-output (SISO) component decoders. The iteration process depends on the first component decoder followed by the second component decoder.

Consider the K-Code channel from 1 to 15 by assigning OVSF code w_1, w_2……w_k and the signaling with additive white Gaussian noise and Multipath channel for the HSDPA turbo system. The block diagram for Turbo HSDPA receiver structure is shown in figure 3. Initially the binary information is encoded using Turbo method for the next iteration. The encoded bits may contain error bursts in the decoder channel input. To reduce the error burst code bit interleaver is used by influencing the each input data bit. The received encoded bits are interleaved for mapping symbol by distributing K code channel to the input bits of the each code. Then the transferred bits are transferred for the next iteration using SF factor by OVSF code spread. For further multipath transmission all the encoded signals are combined and scrambled by aperiodic random code.

The transmission signal is given by

$$x(n) = v(n) \sum_{k=1}^{K} \sum_{i=1}^{M} C_k(i)\, w_k(n - N_c i)$$

Where c_k (n) denotes the data symbol, w_k (n) denotes the OVSF code for code channel, K is the total number of code channels and M is the number of bit/symbols transmitted for each code channel. But the receiver may have the noise in the received signal.

The receiver signal is given by

$$r(n) = \sum_{l=1}^{L_k} h_l x(n - n_l) + \sigma_n(n)$$

Where L_h denotes the multipath channel length

Turbo Iterative model: In the figure-2, turbo iterative structures are shown with ship equalization in the second (lower) half of the figure. It has three stages for signal process: Chip equalizer , SISO multi-code detector , SISO turbo decoder

In HSDPA system, received information has a poor performance Rake receiver by Multi-code interference in the receiver side. To achieve the best performance, Orthogonality property is used by considering partial restoring Channel equalization of spreading waveforms to suppress the MCI. The most advanced technique to increase the performance is Least Minimum Mean Square Error chip equalizer in all chip equalization. The algorithm for Least minimum mean square

chip equalization is determined by

$g = (HH^H+\delta I)^{-1} H\delta_D$

Where δ is noise to signal ratio, δ_D is all zeros except for unity in the $(D+1)$th position, and

$$\boldsymbol{H} = \begin{bmatrix} \hat{h}(0) & 0 & \cdots & 0 \\ \hat{h}(1) & \hat{h}(0) & \ddots & 0 \\ \vdots & \ddots & \ddots & \ddots \\ \hat{h}(L_h-1) & \hat{h}(L_h-2) & \ddots & \hat{h}(0) \\ 0 & \hat{h}(L_h-1) & \ddots & \hat{h}(1) \\ \vdots & \ddots & \ddots & \ddots \\ 0 & 0 & \cdots & \hat{h}(L_h-1) \end{bmatrix}^T$$

By enforcing the above matrix $(HH_H+\delta I)^{-1}$, the major computation is performed by computing coefficients of LMMS chip equalizer. Recursively this matrix inversion is performed by the matrix inversion lemma method. O $((L_h + N_e - 1)^2)$ is the chip equalizer computational complexity where N_e is the length of the equalizer.

The posterior log-likelihood ratio (LLR) of the transmitted signal (whether it is +1 or -1) is delivered by SISO multi-code detector for every code bit of the every code by deciding the priority from the extrinsic information.

Using Bayes' rule

$$\Delta_1[C_k(i)] = \Delta log\frac{P[r(n)|C_k(i)=+1]}{P[r(n)|C_k(i)=-1} + log\frac{P[C_k=+1]}{P[C_k=-1]} = \lambda_1[C_k(i)] + \lambda_2^p[C_k\ (i)]$$

After de-interleaving the output LLR the soft multi-code detector is sent to the turbo decoder. The priori LLR code bits are obtained from the input of the SISO turbo decoder. By decoding the each bit from LLR input the Turbo code structure extrinsic information is collected for the Turbo decoder computation. Since the computation of Turbo decoder to the Turbo decoder standard has the same complexity for each bit of the Turbo SISO decoder. The decoded piori information is processed for next iteration by feedback the output of the SISO Turbo decoder to soft multi-code detector. After the several iteration the hard final decision will be made by computing the information bits of the LLR. The process of how the Decoding process is performed and iteration information identification[12] from the extrinsic information was explained in reference.

HSDPA code detector: The multi-code detection is achieved in HSDPA channel by decoding the extrinsic information of the SISO multi-code detector. In general, the arbitrary multipath delay can be handled by the SISO multi-code detector by simply spreading the multi-path delay for each sample period of the data bit. There may be a poor performance in the receiver side to avoid this performance issue the received signal is bypassed through the Rake receiver and then demodulation is performed in the code bit channel.

The demodulated code bit for the channel is given by

$$y_k(i) = \left\{ h_1^* \sum_{n=N_c i+n_1}^{N_c(i+1)+n_1-1} \begin{bmatrix} w_k(n-N_c i-n_1)v \\ (n-n_1)r(n)z(n-N_c i-n_1) \end{bmatrix} \right\}$$

The Window function z(n) is given by

$$z(n-N_c i-n_1) = \begin{cases} 1 & n \in (N_c i+n_1, N_c(i+1)+n_1-1), \\ 0 & n \notin (N_c i+n_1, N_c(i+1)+n_1-1). \end{cases}$$

From the above obtained value

$$y_k(i) = \left\{ h_1^* \sum_{n=N_c i+n_1}^{N_c(i+1)+n_1-1} \begin{bmatrix} w_k(n-N_c i-n_1)v(n-n_1) \\ r(n)z(n-N_c i-n_1) \\ \sum_{q=1}^{L_h} h_q \sum_{p=1}^{K}\sum_{j=1}^{M} C_p(j).w_p(\\ (n-N_c j-n_q)v(n-n_q)) \end{bmatrix} \right\} + 4\sigma\sqrt{\sum_{i=1}^{L_h}|h_1|^2\ n(i)}$$

In the above equation SISO multi-code detector delivers the decoded extrinsic information.

Low-Complexity HSDPA Multi-Code Detection

In HSDPA system the performance is achieved by reducing the computational complexity of the system by decoding the Turbo multi-code detector. To obtain the low complexity of the system, Soft interference cancellation is implemented based on SISO multi-code detector. By decoding Turbo SISO multi-code detection for the next iteration from the previous iteration we can get the low-complexity and soft estimation of the bit-code[13] with priori LLR extrinsic information.

The received bit-code signal is given by,

$$\hat{C}_k(i) = \sum_{C_k(i)\in\{+1,-1\}} C_k(i)P[C_k(i)] = \tanh\left(\frac{1}{2}\lambda_2^p[C_k(i)]\right), j = 1, \dots, K.$$

After cancelling the soft interference the received signal was transferred for the demodulation, and the received code channel for the bit-code can be written as

$$\hat{C}_k(i) = \sum_{C_k(i)\in\{+1,-1\}} C_k(i)P[C_k(i)] = \tanh\left(\frac{1}{2}\lambda_2^p[C_k(i)]\right), j = 1, \dots, K.$$

And finally the received code channel was demodulated to reduce the soft interference. The process for demodulating the code-channel is given by

$$\hat{y}_k(i) = \sum_{i=1}^{L_h}\left\{h_1^* \sum_{n=N_c i+n_1}^{N_c(i+1)+n_1-1}\left[w_k(n-N_c i-n_1)v(n - n_1)\sum_{p=1}^{K} r_{i,p}(n)z(n-N_c i-n_1)\right]\right\}$$

After demodulation the removed low-complexity soft interference is given by,

$$\lambda_1[C_k(i)] \triangleq log\frac{P[\widetilde{y_k}(i)|C_k(i)=+1]}{P[\widetilde{y_k}(i)|C_k(i)=-1]} = -\frac{|\widetilde{y_k}(i)-\xi_k^+(i)|^2}{32\sigma^2\sum_{i=1}^{L_h}|h_1|^2} + \frac{|\widetilde{y_k}(i)-\xi_k^-(i)|^2}{32\sigma^2\sum_{i=1}^{L_h}|h_1|^2}$$

GPP-Lte Convolution Turbo Code

Single binary Turbo Encoding: A typical single binary Turbo decoder was designed by two identical Recursive systematic Convolutional encoders with separated parallel concatenation of random interleaver.

The recursive systematic Convolutional encoder has the property of half rate code bit. But there is the possibility of 1/3 code bit with the turbo decoder in the received signal for computational complexity as shown in figure 4.

Table-1
LTE Turbo code internal interleave parameters

K	F1	F2
40	3	10
124	103	90
200	13	50
400	151	40
640	39	80
1024	31	64

The received input signal C is transferred to the encoder 1. As per the SISO multi-code detection in the Turbo system the encoded 1 output value is equal to the input of the C block code. The second output in the first parity bit z is encoded by encoder 1. At the same time the second parity bit Z is passed to the Encoder 2 by interleaving the bit code. The main purpose to pass the bit to the Encoder 2 through the interleaver is to avoid the burst error and to increase the performance of the system by increasing the minimum distance of the Turbo codes.

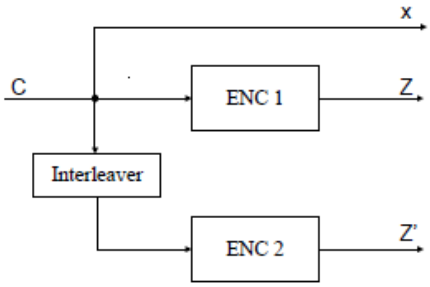

Figure-4
Block diagram of Single Binary CTC Encoder

LTE Encoder: LTE Turbo decoder was designed by employing a Parallel Concatenated Convolutional Code with one internal interleaver by assigning internal interleaver to reduce the burst error along with two constituent encoders by iterative extrinsic information. As we discussed in the previous section about 1/3 coding rate is also explained in figure 5with the Turbo decoder structure

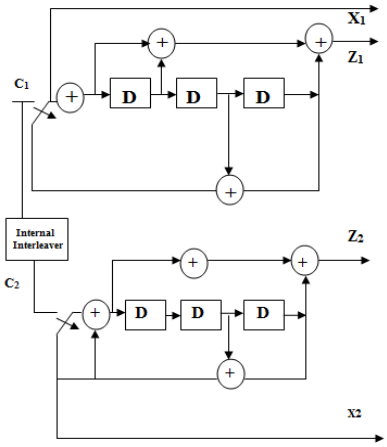

Figure-5
3GPP-LTE CTC encoder

The transformation function of the Turbo decoder for the constituent code is given by

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right]$$

Where $g_1(D) = 1+D^2+D^3$; and $g_0(D) = 1+D+D^3$

Initially the received bits are transferred for decoding process. When decoding the received bits by constituent encoders the initial value for the shift register is assigned to zero. The output from the Turbo decoder is $d_k(0) =$

x_k; $d_k^{(1)} = z_k$; $d_k^{(2)} = z_k$ for k = 0;1;2….k-1. K is the code block size from 40 to 6144 bits.

HSDPA interleaver: From the above decoded function the interleaved Turbo codes are denoted by c_0, c_1, c_{k-1}, where K denotes the number of input bits. The output bits are received after decoding the interleaved output. The input bit and output

bit relationship are given by
$\acute{c}_i = C_{\Pi(i)}, i = 0,1,\ldots . K-1$

The relationship between the input and output index are satisfied and determined by the following quadratic form

$\Pi(i) = (f_1.i + f_2.i^2) mod\ K$

The summarized table for the parameter f_1 and f_2 is given in Table 1

Numerical Results

From the above discussion the simulation output is compared with proposed Turbo iterative receiver and with conventional Rake and Chip equalization for the performance. It is done in HSDPA modulation by employing QPSK modulation, interleaver and Cancelling the Chip equalization. These are achieved by half the bit rate concatenated turbo code value. The recursive polynomial conventional constituent encoded value is generated by

$$G = \frac{n(D)}{d(D)} = (1 + D^4)/(1 + D + D^2 + D^3 + D^4)$$

In the above generated value the channel performance is affected by the mobile velocity in the receiver channel. The Bit error probabilities are evaluated by assigning the mobile velocity in the fading channel. Roll-off factor is employed in the Root cosine pulse by using the QPSK modulation. And the chip equalization bit rate is assigned to megabyte range. In the table 1 the different channel modes for the two Rayleigh fading channels are given. In the two channels there is a week propagation path for path for data transfer. To address this week propagation path Channel II path is added to the channel I path [12] and the propagation path was removed from the above addition.

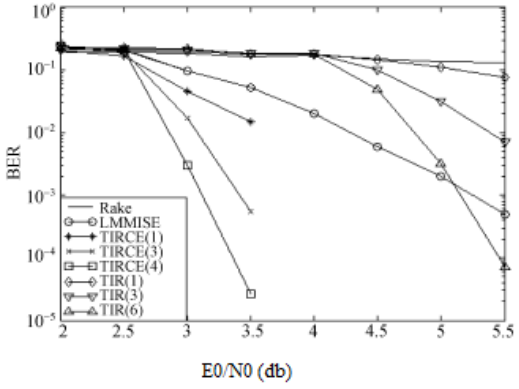

Figure-6
HSDPA BER curves versus energy contrast E_0/N_0

There are so many channels factors for the multi code channel is evaluated in figure 6. In the above figure the comparison is between the HSDPA bit error rate (BER) and energy contrast (E_0/N_0) in the channel II. From the above comparison the results are compared with the presence of MPI and MCI is as expected. In the result the performance of the Rake receiver is very poor. But the performance of the Turbo iterative receiver is very high in the conventional decoder receiver. The chip equalization selection for SNR is calculated based on the chip equalizer outgoes. Based on the outgoes the Turbo iterative receiver selects without chip equalization for low SNR and with chip equalization for high SNR.

Conclusion

From the above discussion, the HSDPA system is yielding the poor performance in the multi-code interference which is caused by the Rake receiver in the multipath. To avoid this poor performance we proposed the modified HSDPA system structure. In this structure there is the modification in SISO multi code detector and SISO turbo decoding. The design is done by combining the SISO Turbo decoder and SISO detector with Chip equalization. In this modified structure the receiver performs well with low power distortion especially multi code channel for high speed data rate transmission. Further improving the Turbo multi-code detection is implemented in Chip equalization the performance was increased.

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