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Novel Characteristics of Junction less Dual Metal Cylindrical Surround Gate (JLDM CSG) MOSFETs

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Abstract

After the fabrication of a junction less (JL) transistor by the Colinge et al at Tyndall National Institute, it is now considered a substitute for the junction transistors at highly scaled dimensions. One of the biggest advantages reported is its current driving capability. Being a depletion mode device it is normally ON device and has to be switched OFF by applying a certain gate voltage. In this paper we have explored some novel characteristics of a junction less dual metal (JLDM) CSG MOSFET using 3D numerical simulations and compared it with a standard JL single metal (JLSM) transistor of identical dimensions. Some interesting properties of the JLDM has been revealed not reported earlier. Many analog and RF performance parameters of JLDM such as transconductance g_m*, TGF* g_m/I_D*, early voltage* V_{EA}*, unit-gain cutoff frequency* f_T*, maximum frequency of oscillation* f_{MAX}*, gain bandwidth product (GBW) etc. have been observed to have improved values as compared to the JLSM.*

Keywords: Junction less, dual metal gate, cylindrical surrounding gate, analog, RF, numerical simulation.

Introduction

Due to the aggressive scaling of transistor these has become of nanometer sizes. At these sizes it is very hard to control the sharp source/drain-channel junctions' from the device fabrication point of view. Also many other unwanted deleterious effects such as gate leakage, short channel effects (SCEs), hot carrier effects (HCEs) etc. have been seen to be increasing. For reducing the short channel effects the gate all around MOSFETs are the best since these provide best control over the channel from all around. But if we use channel with corners (i.e. rectangular shape) for this purpose then it leads another effect known as corner effect. To avoid this, cylindrical structure looks to be promising and has been widely used for getting rid of corner effect and also to improve other SCE performance parameters.

For enhancing the carrier transports in the channel and reduce the hot carrier effects (HCEs) a dual metal gate structure has already been studied theoretically[1-4] and some fabrication methods[4-7] suggested in literature for the conventional MOSFETs. The dual metal structure improves these by modifying the electric field component along the channel and modifying the potential distribution in the channel[2,5,8]. The dual metal gate structure has been reported to be fabricated by tilt angle evaporation[5], metal inter diffusion[9] and metal wet etch process[10]. Combining the dual metal and cylindrical surrounding gate structures has been proposed to be incorporated with the junction less transistors by Haijun Lou et al[11].

Junctionless (JL) transistors are inherently depletion mode devices and needs a gate voltage to be applied to make them OFF[12-17]. One advantage of these are that it operates due to the conduction of carriers in bulk as opposed to the conventional MOSFETs (inversion mode devices) in which the carriers conducts through a thin layer of inversion charge layer create at the oxide/semiconductor interface. Hence, the current driving capability is improved a lot however it is also degraded slightly due to the high doping concentrations used in the channel. Hajun et al has reported many interesting properties of this Junctionless dual metal cylindrical surrounding gate (JLDM CSG) MOSFET by 3D numerical simulations however there are still many other properties associated with the analog and RF performance remains to be explored. Recently some models of JL transistors have also been reported[18].

In this paper we have performed 3D numerical simulations using the Sentaurus TCAD and effect of control gate ratio (ratio of the dual metal gate lengths) on transconductance g_m, intrinsic gain g_m/g_d, TGF g_m/I_D, early voltage V_{EA}, gate capacitance C_{gg}, gate drain capacitance C_{gd}, unit-gain cutoff frequency f_T, maximum frequency of oscillation f_{MAX}, gain bandwidth product (GBW) etc. has been explored. The above performance parameters are also compared with a standard Junctionless single metal cylindrical surrounding gate (JLSM CSG) MOSFET of identical dimensions.

The paper is arranged in following parts. First part covers the introduction followed by methodology which describes the JLDM-CSG MOSFET structure formation. After this we have

results and discussion section in which the JLDM and JLSM are compared for the analog, electrical and current voltage characteristics. In last section the conclusions are drawn resulted due to the numerical simulations of the JLDM.

Methodology

Device structure Generation of the Junctionless Dual Metal Cylindrical Surrounding Gate MOSFETs: Figure-1 shows the 3D structure of a typical Junctionless dual metal cylindrical surround gate (JLDM CSG) MOSFET with $L1 = L2 = 15nm$ and $R = 5nm$. Highly doped silicon with $2.0\times10^{+19} cm^{-3}$ (arsenic) was used as source/drain and channel regions. The two laterally contacting gate materials for dual metal used are titanium ($\phi_{M2} = 4.4eV$) and Aluminum ($\phi_{M3} = 4.1eV$) respectively. The gate oxide thickness (SiO_2) has been taken to be $1nm$ for all the devices under consideration so that there is no gate tunnel current. The results of JLDM has been compared with a typical Junction less single metal (JLSM) CSG MOSFET of gate length $30nm$ (titanium) with all other device parameters taken to be identical.

The device has been simulated using 3D device simulations using Sentaurus Device tool of Synopsys Sentaurus TCAD[19]. Poisson's equations with density gradient models have been solved for the JLDM and JLSM CSG MOSFETs. Density gradient quantization models can be used for the simulations of quantum wells, SOI structures and MOSFETs to get reasonable description of terminal characteristics.

These devices are first simulated to get the DC and analog characteristics and then ac simulations have been carried out to extract the RF characteristics.

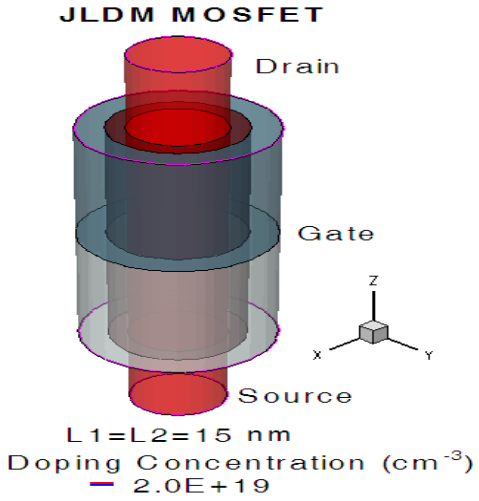


Figure-1
Structure of Junctionless Dual Metal Cylindrical Surrounding Gate Metal Oxide Semiconductor Field Effect Transistor (JLDM CSG MOSFET)

Results and Discussion

Electrical and Current Voltage Characteristics: The electrostatic characteristics of JLDM are shown in the figure-2 for $V_{GS} = 1.0V$ and $V_{DS} = 1.0V$. Figure-2(a) and (b) represent the electrostatic potential at the SiO_2/Si surface and in the center of the channel respectively. Potential at the surface is larger as compared to the center. Electric field variations shown in the figure-2(c) are slightly more for JLDM at source side whereas it is less on the drain side. Due to larger electric field on the source side the electrons injection into the channel, as shown in figure-2(d), from source will be with a larger velocity as compared to the JLSM and simultaneously it will also reduce the hot carrier effects to some extent due to reduced field on the drain side. There is also a peak in the electric field seen due to the dual metal structure of JLDM. The electron density is also larger as compared to the JLSM as shown in the figure-2(e).

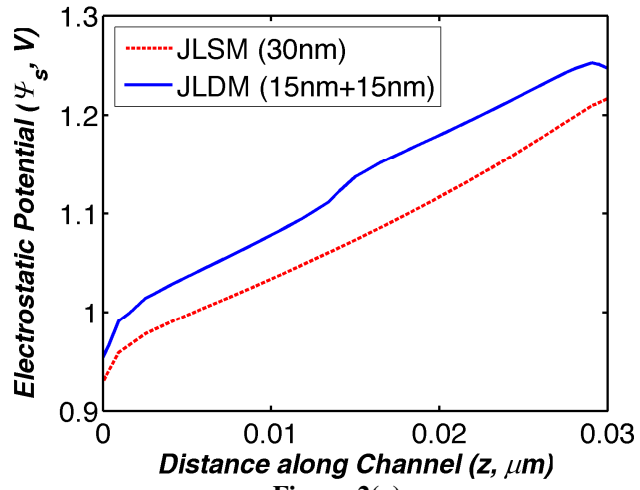


Figure-2(a)
Surface Electrostatic potential (Ψ_s)

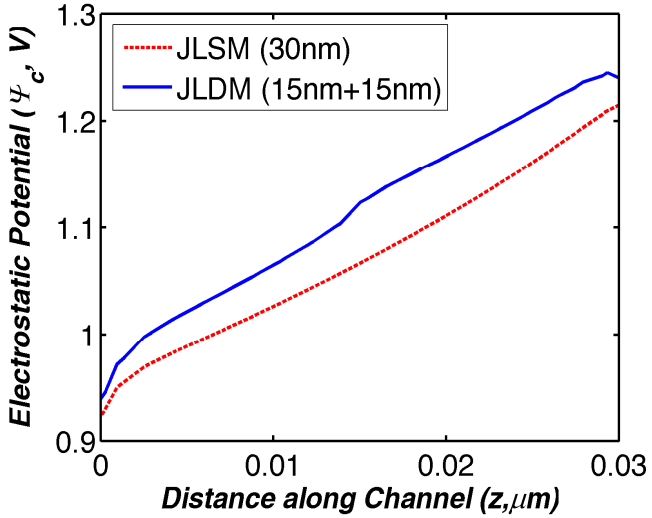


Figure-2(b)
Electrostatic potential in the center (Ψ_c)

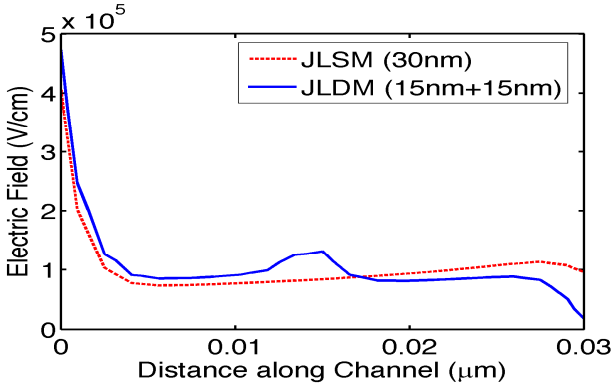


Figure-2 (c)
Electric field

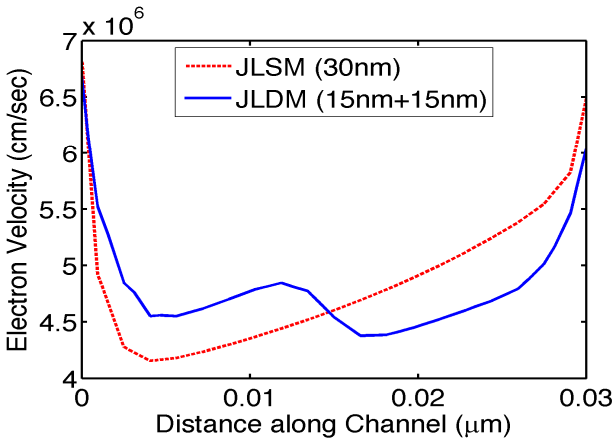


Figure-2 (d)
Electron velocity

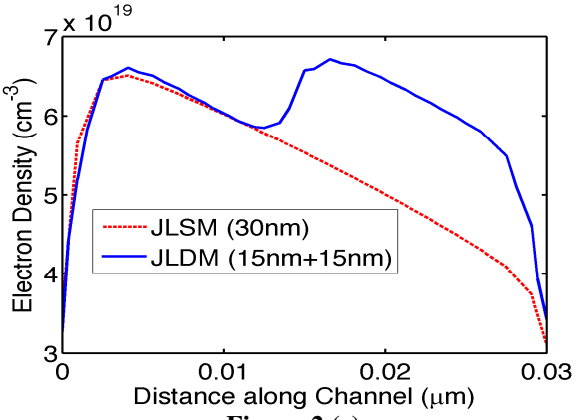


Figure-2 (e)
Electron density at SiO_2/Si interface for $V_{GS}=1.0V$ and $V_{DS}=1.0V$

The DC current voltage characteristics are shown in Figure-3(a) and (b) respectively at $V_{DS}=1.0V$. ON state current is slightly higher for the JLDM as compared to the JLSM. This increase in the current is obtained due to the dual metal structure used. This is due to the presence of high horizontal component of electric field at the source side which improves the injection velocity of the electrons injected.

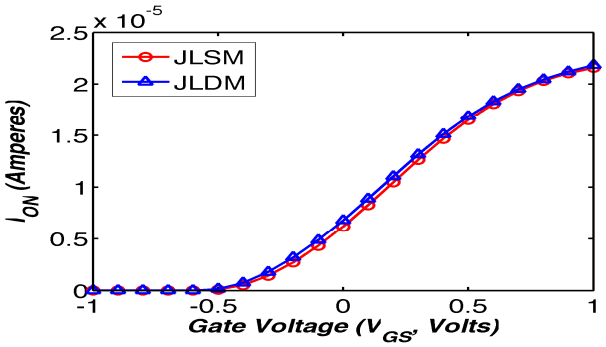
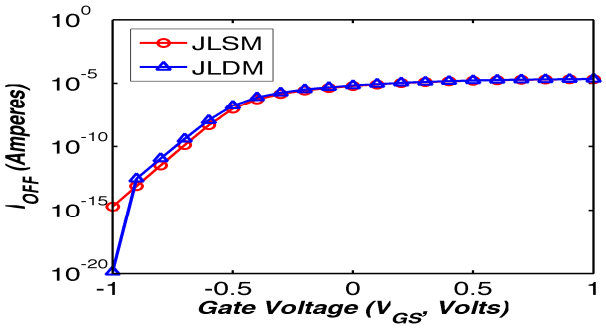


Figure-3(a)
ON state current $(V_{DS}=1.0V)$



(b)

Figure-3 (b)
OFF state current $(V_{GS}=0.0V)$

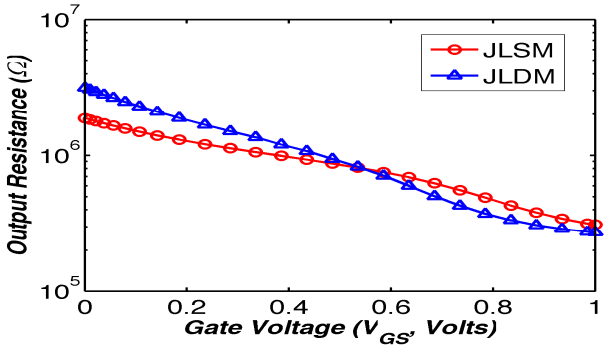


Figure-4(a)
Output resistance (R_o)

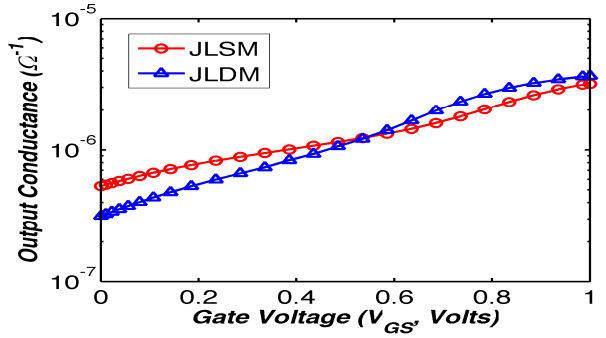


Figure-4(b)
Conductance (g_d) $(V_{DS}=1.0V)$

Figure-4(a) and (b) reports the output resistance and conductance respectively. The output resistance is higher in subthreshold regime (below $\approx 0.5V$) and is lower in super threshold regime (above $\approx 0.5V$). Similarly, the conductance varies inversely to the variation of the output conductance.

Analog and RF characteristics: Next, we discuss the analog performance parameters e.g. transconductance g_m, intrinsic gain g_m/g_d, transconductance generation factor (TGF), early voltage V_{EA}, etc. Transconductance is very important analog parameter and is defined by

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS}} \quad (1)$$

Transconductance g_m is lower for the JLDM as shown in figure-5(a). Intrinsic gain is the available gain of a transistor and is shown in figure-5(b). The intrinsic gain is also lower due to the lower g_m. The TGF is the available gain per unit of power dissipation and is shown in the Figure-5(c). The TGF is also lower for the JLDM as compared to the JLSM. The early voltage as shown in Figure-5(d) is also lower for the JLDM. This comparison shows that the JLDM is not performing better as compared to JLSM in terms of the analog performance parameters.

Now, let us look at the RF performance parameter variations. In Figure-6, C_{gg} and C_{gd} have been compared, which are important parameters for determining the frequency response of a transistor. Both capacitances are higher for the JLDM as compared to the JLSM, which will deteriorate the frequency response.

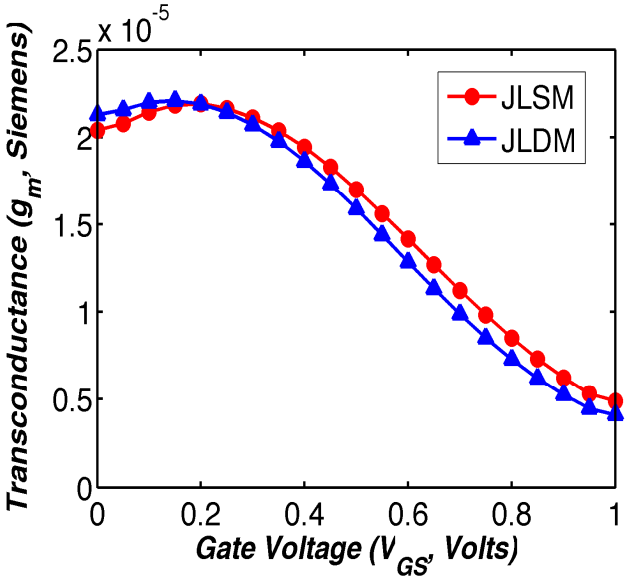


Figure-5(a)
Transconductance (g_m)

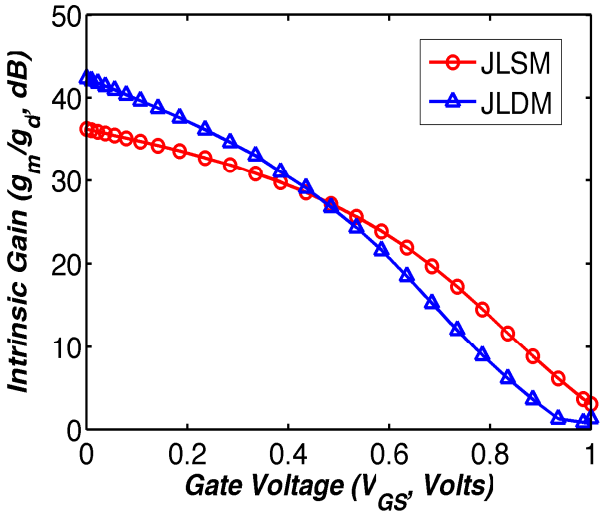


Figure-5(b)
Intrinsic gain $(g_m R_o \; or \; g_m/g_d)$

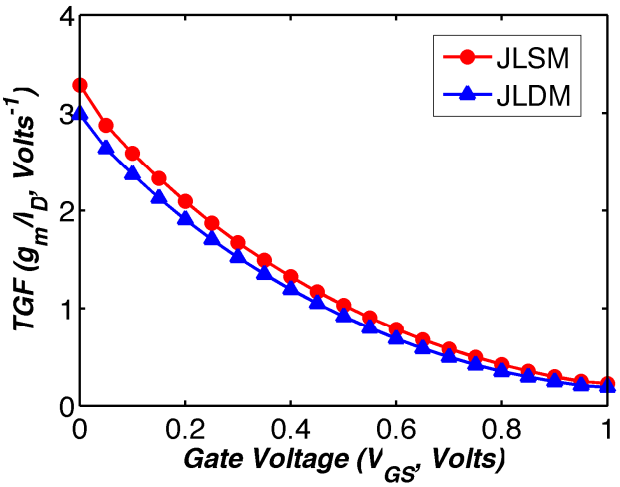


Figure-5(c)
Transconductance generation factor $(TGF, g_m/I_D)$

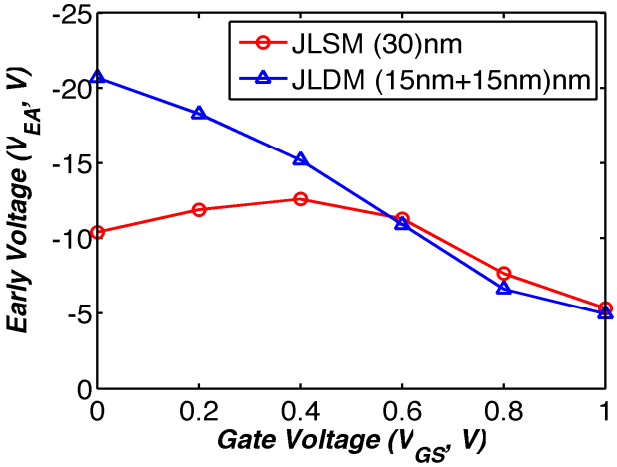


Figure-5(d)
Early voltage (V_{EA}) **at** $(V_{DS} = 1.0V)$

The other important RF performance parameters are the cutoff frequency (f_T), maximum frequency of oscillation (f_{MAX}) and gain bandwidth product (GBW). The f_T is defined as the frequency at which the short circuit current gain decreases to unity (sometimes referred as the transition frequency), and is given by

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (2)$$

Where g_m is the transconductance and C_{gg} is the gate capacitance. The f_{MAX} is the frequency at which the power gain becomes unity and is given by

$$f_{MAX} = \frac{g_m}{2\pi C_{gs}\sqrt{4\left(g_{ds} + g_m \frac{C_{gd}}{C_{gs}}\right)\left(R_s + R_{ch} + R_g\right)}} \quad (3)$$

Where C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitances respectively, g_{ds} is the output conductance, R_s - source resistance, R_{ch} - channel resistance, and R_g - gate resistance.

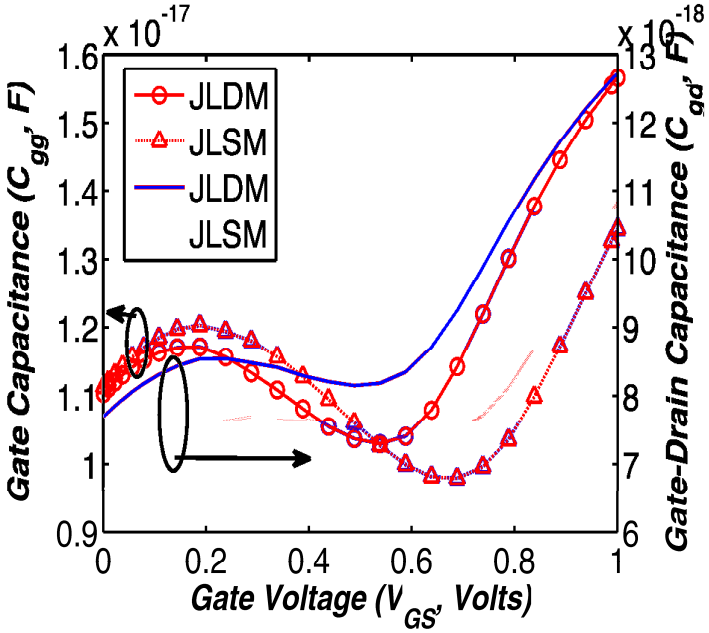


Figure-6

Gate capacitance (C_{gg}) and Gate-Drain capacitance (C_{gd})

For the extraction of these parameters ac analysis is performed over a frequency range (here $1\times10^6\ Hz$ to $1\times10^{13}\ Hz$) and Y parameters are computed. After this two port network RF extraction tool (Inspect from Synopsys Sentaurus TCAD) is used to compute the f_T and f_{MAX} using the following equations[20]-

$$f_T = f_i.|H_{21}| \quad (4)$$

$$f_{MAX} = f_i.\left[\frac{|Y_{21} - Y_{12}|^2}{4\left[\mathrm{Re}(Y_{11}).\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{21}).\mathrm{Re}(Y_{12})\right]}\right]^{\frac{1}{2}} \quad (5)$$

Where f_i is the input signal frequency.

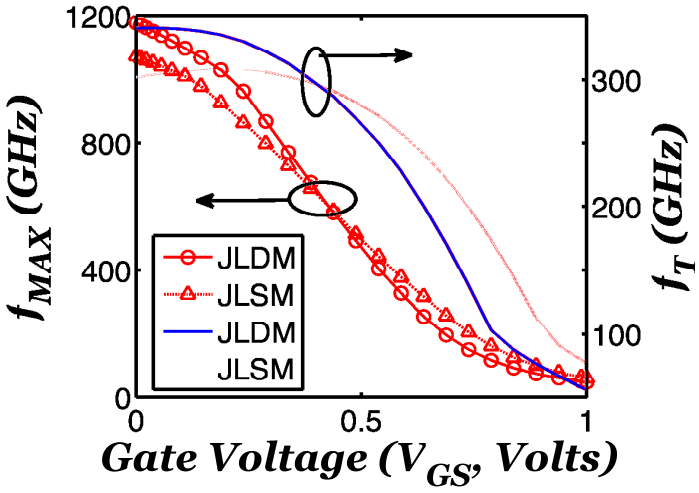
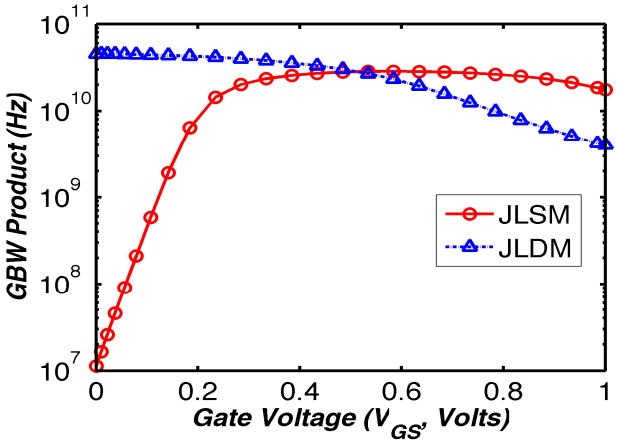


Figure-7(a)
Maximum frequency of oscillation (f_{MAX}) and cutoff frequency (f_T)



(b)

Figure-7
Gain band width (GBW) product

The GBW is shown for both the MOSFETs in Figure-7(b), which is computed by the following approximate equation

$$GBW = \frac{g_m}{2\pi.10.C_{gd}} \quad (6)$$

The GBW is slightly lower for the TMCSG due to larger C_{gd}.

The transition frequency f_T and maximum frequency of oscillation f_{MAX} is shown in figure-7(a). As expected, both of the above parameters are degraded for the JLDM. The gain band width product shown in figure-7(b) is also degraded in the super threshold region of operation. Whereas all the above stated

performance parameters are better as compared to JLSM in the subthreshold region of operation. The simulation results provide an opportunity to the JLDM to be explored and used in the subthreshold region of operation. Thus it seems to be a promising candidate for the low voltage and low power applications.

Variation of different performance parameters due to control gate ratio: In this section, the JLDM is explored with varied $L1:L2$ ratio (gate length ratio) ranging from 1:5 to 5:1for a total gate length of $30nm$. The surface electrostatic potential (Ψ_s) and electrostatic potential in center (Ψ_c) as shown in figure-8(a) and (b) respectively, is larger for the 1:5 gate length ratio near the source region representing a larger concentration of electrons (figure-8(e)). The electron velocity and the horizontal component of the elctric field near the source region are also higher for the 1:5 gate length ratio as shown in Figure-8(c) and (d) respectively. This is due to the larger length of the second lateral gate $(L2)$ which screens the effects of the drain voltage variations (absorbs extra voltages than the threshold voltage). This in turn leaves the current to control lesser charges which in turn increases the channel potential. The analog performance parameters Transconductance (g_m), Intrinsic gain $(g_m R_o \, or \, g_m/g_d)$, Transconductance generation factor $(TGF, g_m/I_D)$ and Early voltage (V_{EA}) are shown as in figure-8(a), (b), (c) and (d) respectively. The close investigation of the variations of above mentioned parameters reveals that the analog performance parameters are worst for the 1:5 gate length ratios whereas it is better for the 5:1 gate length ratio. The $I_D - V_{GS}$ curves have been plotted in the figure-9(f). It can be seen that for lower $L1/L2$ (gate control) ratio the current is larger and it decreases with the gate control ratio increase.

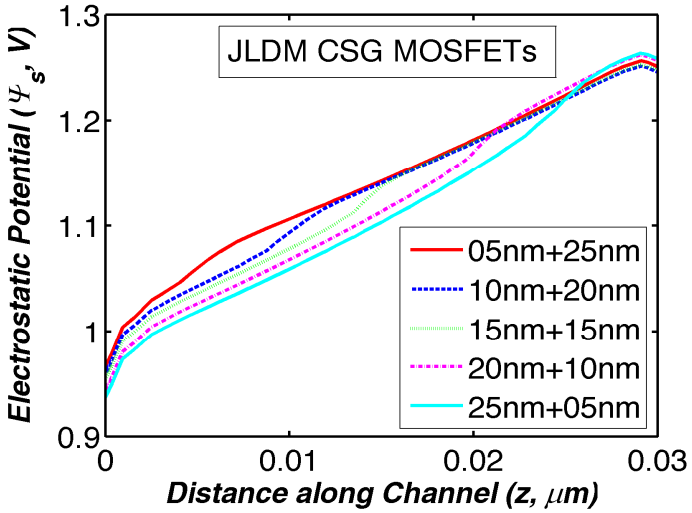


Figure-8(a)
Surface Electrostatic potential (Ψ_s)

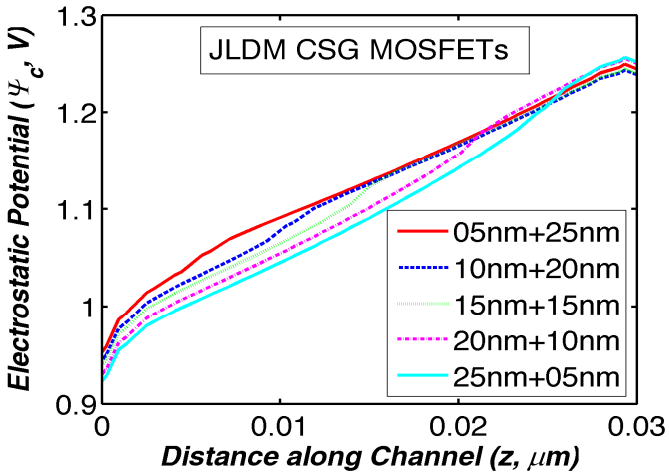


Figure-8(b)
Electrostatic potential in the center of (Ψ_c)

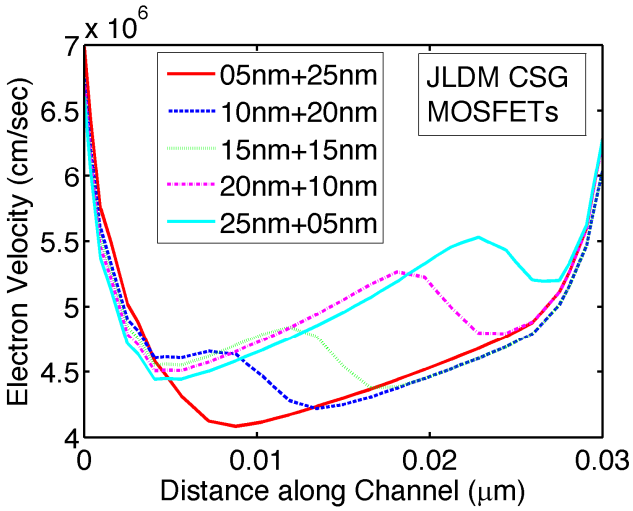


Figure-8(c)
Electric field

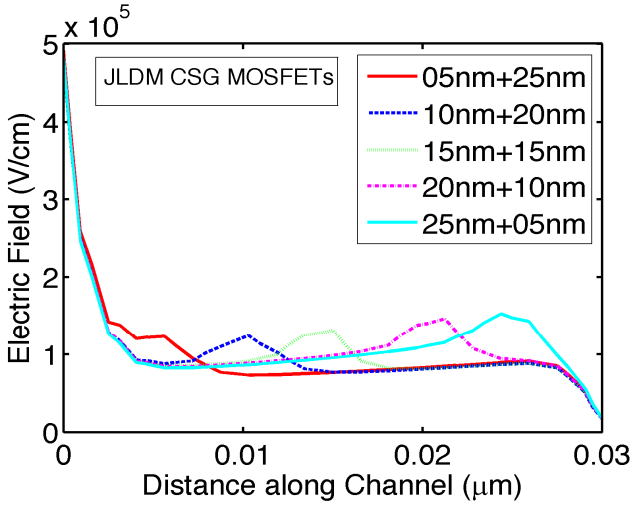


Figure-8(d)
Electron velocity

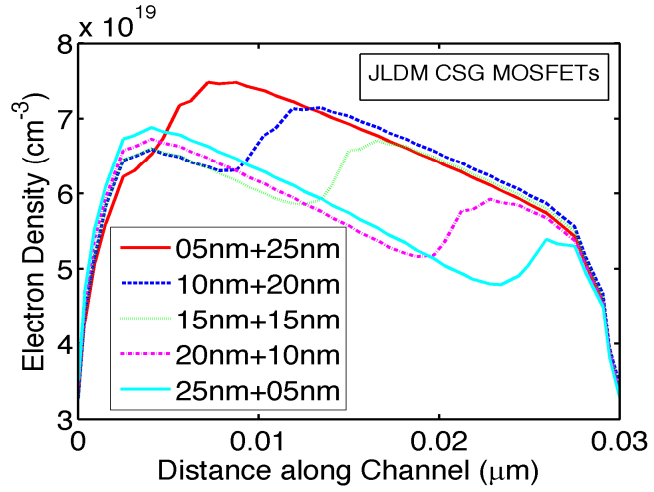


Figure-8(e)

Electron density at $V_{GS}=1.0V$ and $V_{DS}=1.0V$

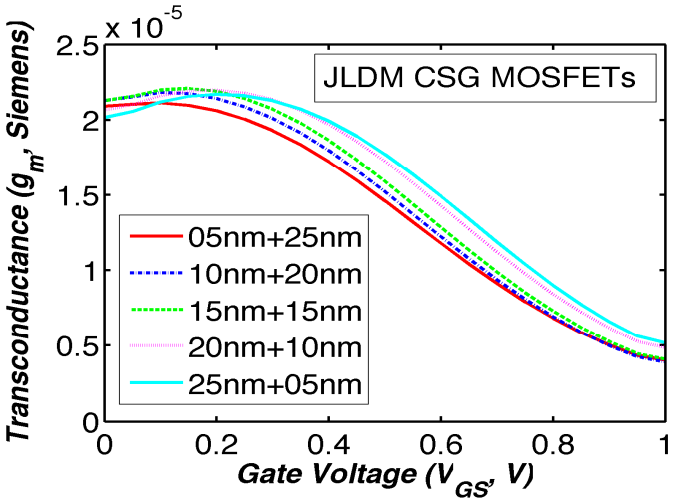


Figure-9(a)

Transconductance (g_m)

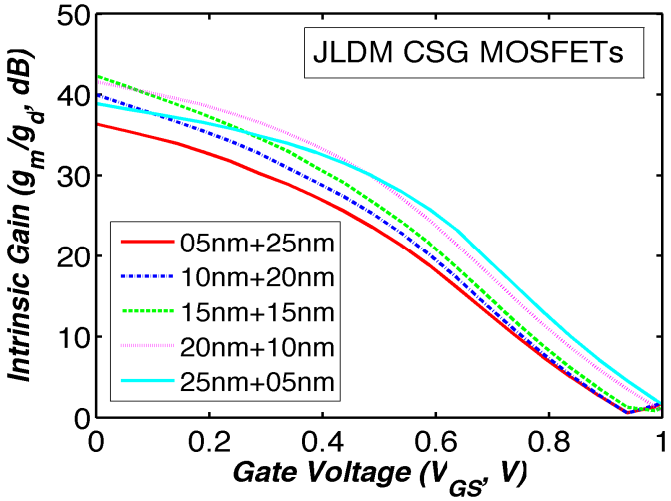


Figure-9(b)

Intrinsic gain $(g_m R_o \text{ or } g_m/g_d)$

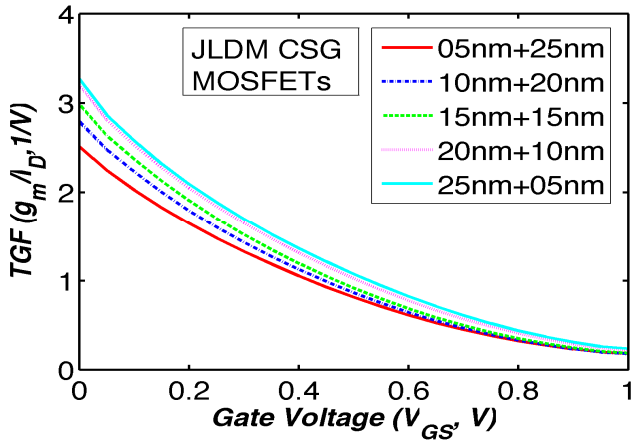


Figure-9(c)

Transconductance generation factor $(TGF, g_m/I_D)$

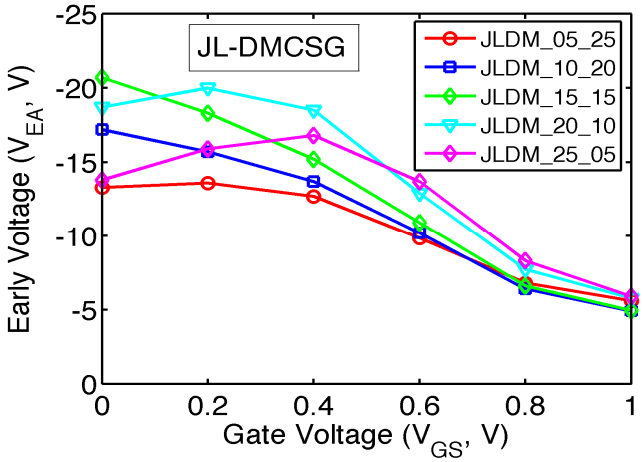


Figure-9(d)

Early voltage (V_{EA}) at $(V_{DS}=1.0V)$

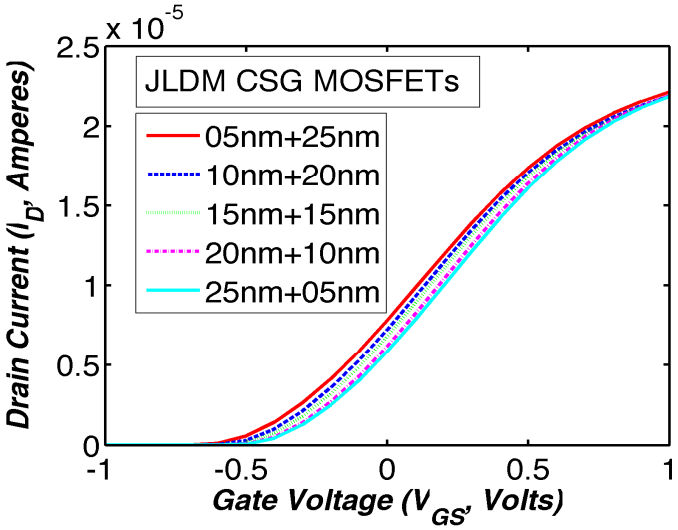


Figure-9(e)

$I_D - V_{GS}$ curves

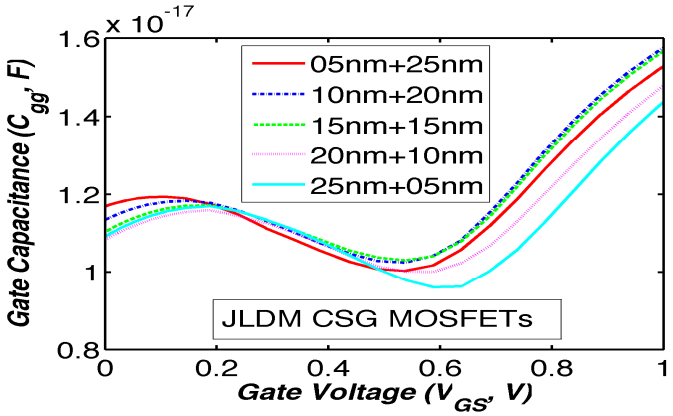


Figure-10(a)
Gate capacitance (C_{gg})

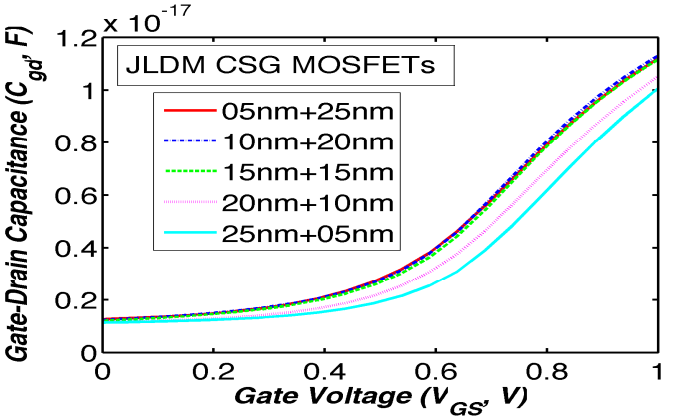


Figure-10(b)
Gate-Drain capacitance (C_{gd})

The gate capacitance C_{gg} and gate-drain capacitance C_{gd} are shown in the figure-10(a) and (b) respectively. C_{gg} is lower for the 5:1 and is highest for the 1:1 gate length ratio. Similarly, C_{gd} is also larger for the 1:1 and lower for the 5:1 gate length ratio. This is due to the reason that the area under the gate *L2* is mostly depleted which becomes in series with the gate capacitance (C_{ox}) and hence lowers overall capacitance whereas the area under the gate *L1* is only due to the C_{ox} which is constant.

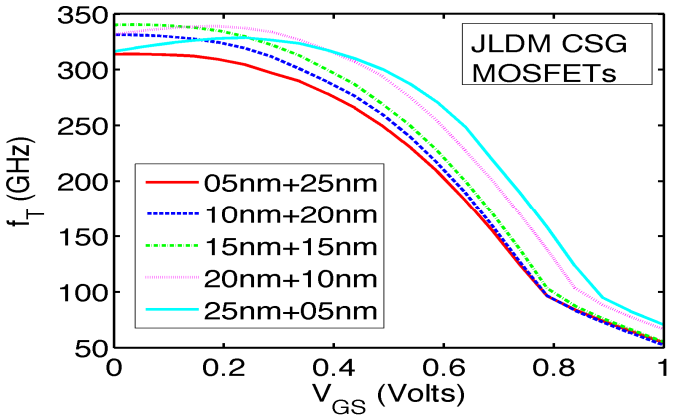


Figure-11(a)
Cutoff frequency (f_T)

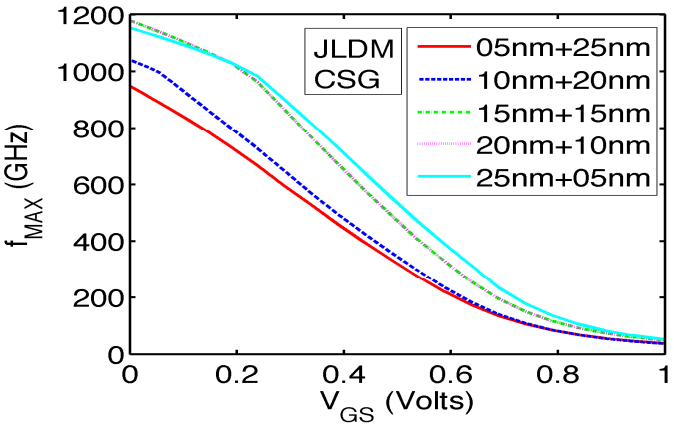


Figure-11(b)
Maximum frequency of oscillation (f_{MAX})

The cutoff frequency (f_T) and maximum frequency of oscillation (f_{MAX}) are shown in the figure-11(a) and (b) respectively. f_T and f_{MAX} both are higher for the 5:1 gate length ratio due to smaller values of C_{gg} and C_{gd}. The GBW is also higher for the 5:1 gate length ratio as shown in figure-12.

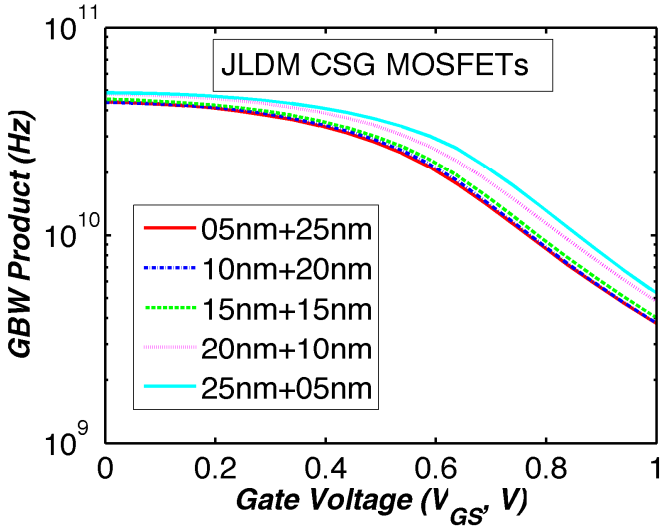


Figure-12
Gain band width (GBW) product

Conclusion

Since the JLDM MOSFETs are normally ON transistor similar to JLSM at zero gate potential, a negative potential (for n-channel) is required in order to switch it OFF. This will certainly increase the power requirements of the circuit. However, the simulations show a slight degradation in the analog and RF performance parameters in the strong inversion regime of operation, the JLDM provides better performance in the subthreshold regime. The study discloses the fact that JLDM transistors may be used for low power analog/RF applications

whereas it may not be suitable for the digital applications since this does not provide very high I_{ON}/I_{OFF} ratio. It may also be suitable to be used for low power applications as well. The fabrication of the JLDM transistors can be done using the traditional methods of fabricating the junction transistors with less number of processing steps.

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