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Implementation of LOSSY image compression by discrete wavelet transform

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Abstract

The discrete wavelet transform (DWT) represents images as a sum of wavelet functions (wavelets) on different resolution levels. The wavelet transform can be composed of any function that satisfies requirements of multiresolution analysis and exists a large selection of wavelet families depending on the choice of wavelet function. The choice of wavelet family depends on the application. In image compression application this choice depends on image type. A fundamental shift in the image compression approach came after the Discrete Wavelet Transform (DWT) is growing fast. In this paper, the design of DWT with new Vedic multiplier is presented in 2d-DWT structure, Digital FIR filter is used to increase the image resolution and remove the unwanted noise present in the image. This research work presents the efficiency of Urdhva Triyagbhyam Vedic method for multiplication which strikes a difference in actual process of multiplication itself. Multiply Accumulate unit (MAC) is a key component in the most of the digital signal processors, in order to make a balance in the key performance characters like speed, power and area, a gate level implementation of the design is adopted in the entire research work.

Keywords: Discrete wavelet transform, PSNR, image quality, image reconstruction, vedic multiplication, Kogge stone adder.

Introduction

The Wavelet transform holds each time and frequency facts, based on a multi-resolution analysis framework while as compared to conventional transforms like fast Fourier Transform (FFT) and the Discrete Cosine Transform (DCT)[1]. Wavelet Transform has been used in many fields, which include photo and sign processing, sign compression, inter-stellar information evaluation, virtual fingerprints, noise reduction and so on. Data compression is a technique which has used for compress any image, video or text for transfer with less bandwidth consumption. This paper is focusing on image compression which can be define as a technique for compress lossy or lossless image using DWT. Image compression also used for reduce the redundancy of input image for transmit date in an efficient form[2]. DWT design required for reduce the storage and better rate of transfer. This is a new technique and having many advantages as compare to other technique like its large variety of decomposition of images[3].

Computation Scheme for DWT: The functionality of discrete wavelet transform is defined in computation of input signal. The input signal or image signal has decomposed into two part or sub-band which is called as low-pass sub-band and high-pass sub-band. These low-pass sub-band and high-pass sub-band are used for filtering the input signal of DWT decomposition. As per Figure-1, the LPF and HPF are short length finite impulse response (FIR) filter. Both filter has been down sampled to obtain low pass and high pass output $u_h(n)$ and $u_l(n)$ and it is called Filtering Unit[4].

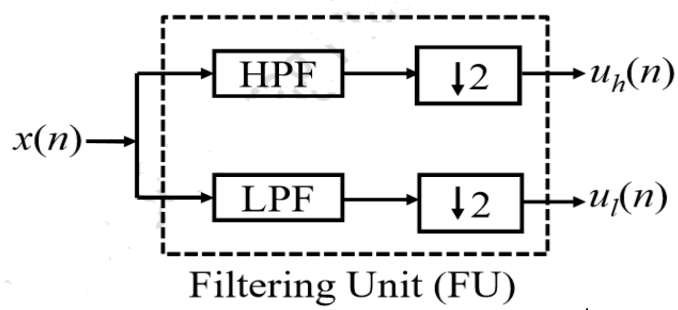

Figure-1: Computation of one level 1-D DWT[4].

As per Figure-2, the Input signal or image signal would be decompose by 3-levels. For example the original input signal x[n] having N samples and after 1-level it would be divide as N/2 samples then N/4 and N/8 by 2nd and 3rd level decomposition of input signal. In terms of image if input signal having 512 sample point and frequency band of 0 to π rad/s then after first decomposition of signal the output of high pass and low pass filters would be 256 sample and frequency band of π/2 to π rad/s because of double frequency resolution. The information of Low pass filter is more impotent then high pass filter then again this 256 sample will pass to DWT and output would be 128 samples and so on[5].

Pyramid algorithm (PA) algorithm is proposed for repeating the DWT level and parallel computation of multilevel DWT that is called Mallet wavelet algorithm and PA for 1-D DWT has shown by Figure-3.

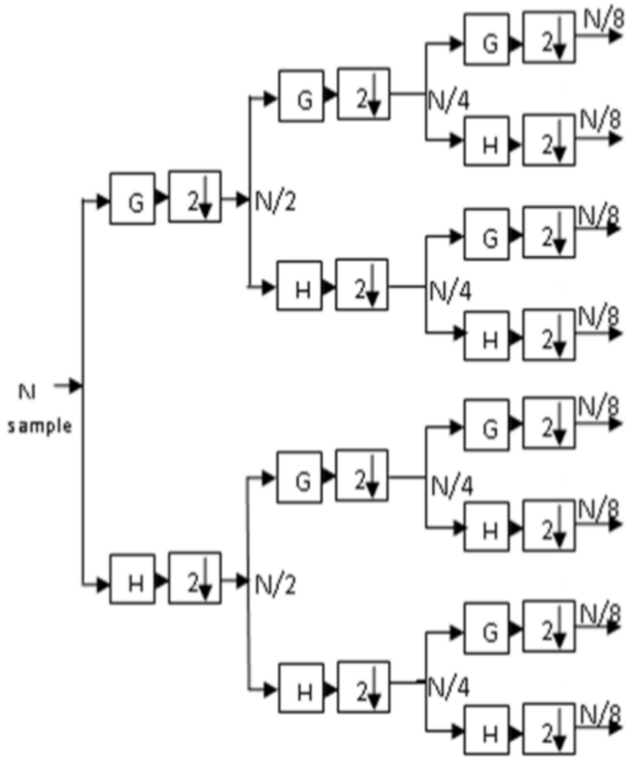

Figure-2: 3-levels for 2-D DWT where G and H are the high-pass and low-pass filters respectively[5].

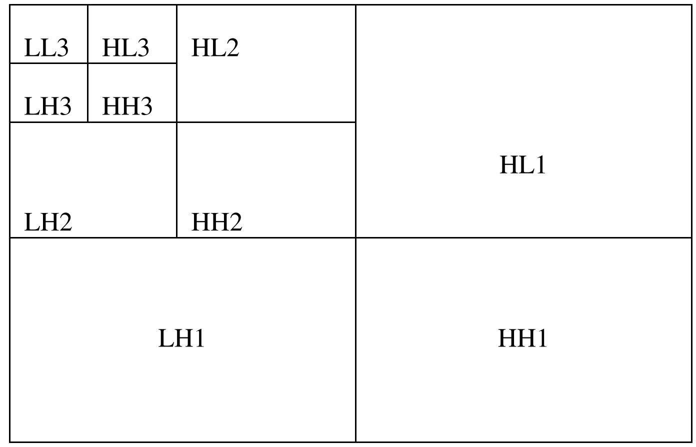

Figure-3: Three Level Diagram of Low High Filter Bank.

Vedic Multiplier using KS Adder: Vedic multiplier and Kogge-Stone can compare with conventional method which is computed by Vedic multiplier, full adder and half adder. Proposed technique provides less path delay and less area. Input sequence of Conventional method is much more than to proposed method, however proposed method has less propagation delay. Area and propagation delay can be reduced by the aid of modified KS adder. This adder will be designed like as ripple carry adder[6]. Carry output of one KS adder is connected with another KS adder but this method is very beneficiary for high efficient digital devices as per concerning propagation delay[7].

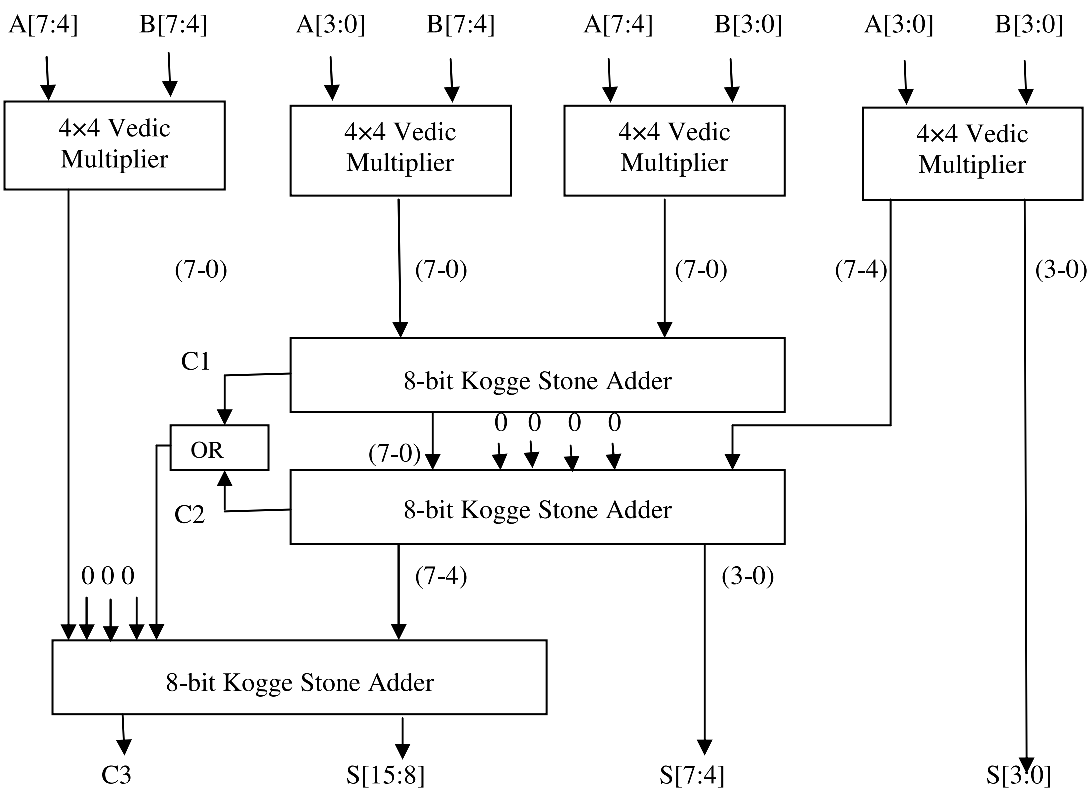

Figure-4: Logic Diagram of Vedic Multiplier using Kogge Stone Adder.

Methodology

Wavelets could be used to compress and improving signal quality in the field of medical image. This image has requires very fine image resolution scale with very less noise.

2D wavelet have image of horizontal and vertical dimensions and it analyses in both way. For analyzing any signal generally wavelet follow mother wavelets but image compression it requires compression on every level. As per Figure-5, the input image having matrix of m×n. In the decomposition of image signal, image would be compress in terms of low and high filter combination. By which the output image would be divide in four sub-image. The analysis of wavelet transform using Vedic multiplier give change of image in vertically, horizontally and diagonally.

For the next level of decomposition the image has decomposed, as per Figure-6. Compression and decompression has been done by encoder and decoder simultaneously but encoder consists of three blocks and other one decoder having two blocks as per Figure-7.

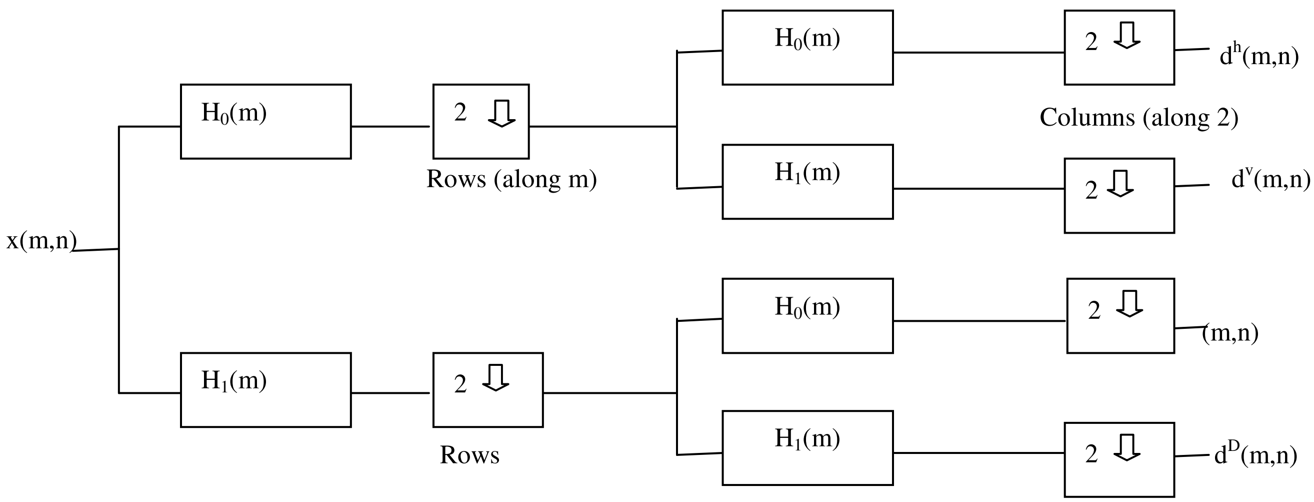

Figure-5: 2D wavelet analysis of an image.

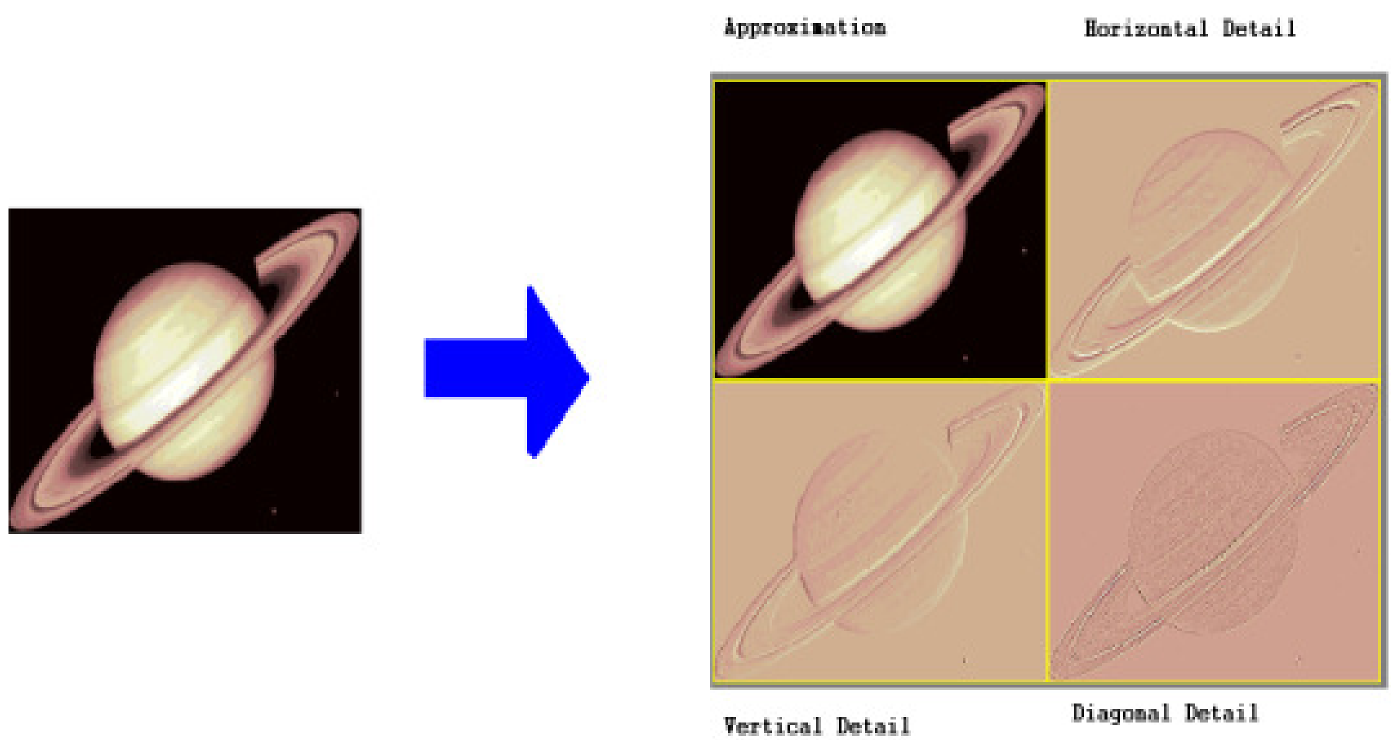

Figure-6: 2D decomposition of Saturn image in level 1.

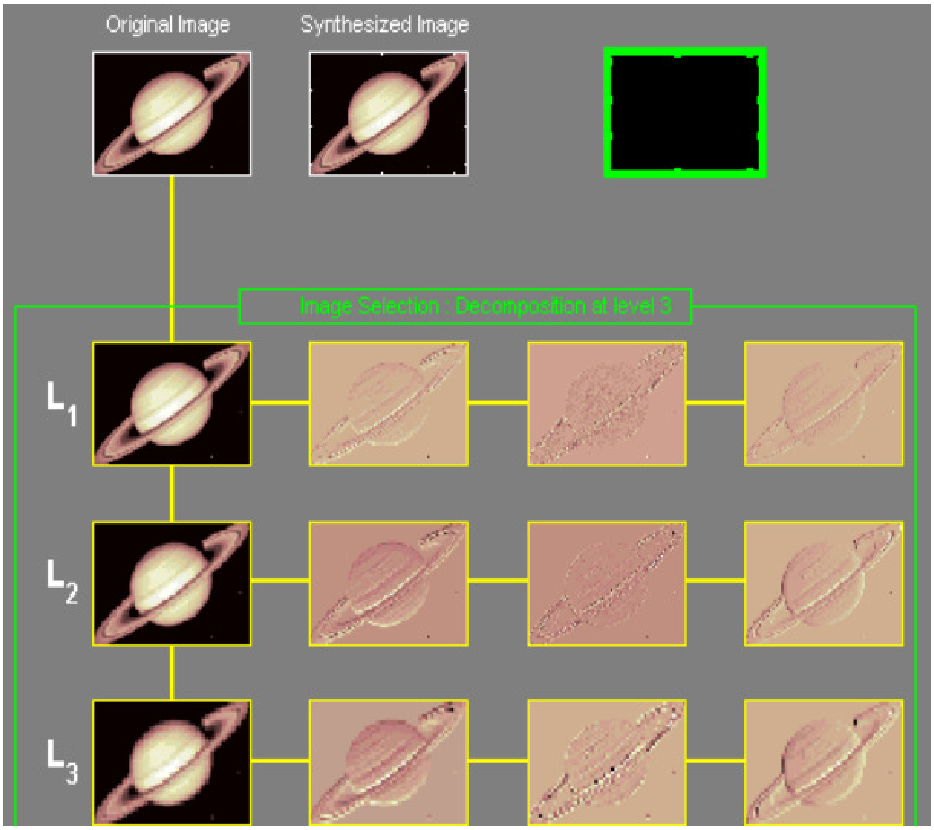

Figure-7: Saturn image decomposed to level 3.

First stage encoding process has done by Mapper transforms f(x, y) for decreasing redundancy of inter pixel and operation has reverse as well as length coding has run by this. For second stage quantizer fetched usefull information. This compressed image is called lossy compression. The last and final stage of encoding is generate variable or fixed length code to present quantized output. This variable code is generally use to decrease the coding redundancy and it might be reversible.

Above algorithm illustrates the general process of image compression: i. Take any Size of input image; here we have taken grey scale image. ii. Divide image into 16 by 16 blocks. iii. Works from top to bottom and left to right DCT is applied to each block. iv. Each block then compressed using quantization. v. The array obtained from the quantization of each block have reduced amount of data and compressed image is reconstructed using decompression.

Results and discussion

We have implemented the proposed Vedic Multiplier using Kogge stone adder base on digital circuit. Basic architecture of Vedic multiplier Consists of full adder and half adder which requires less time to compute result. We have device summary of proposed multiplier and existing algorithm to achieve good computation speed compare to other shows in Table-1 and Table-2. Show the bar graph of the proposed design in Figure-8 and Figure-9 respectively.

Table-1: Comparisons Result for proposed design and existing algorithm

Design	Width	Area court
BEC Based Adder	8	188
	16	376
	32	752
CSLA Adder	8	133
	16	266
	32	532
G. R. Gokhale[6]	8	104
	16	208
	32	416
Proposed Adder	8	82
	16	164
	32	329

Table-2: Device utilization summary of 8-bit Vedic Multiplier.

Design	Width	Area count	MCPD
B. K. Mohanti[4]	8-bit	1545	41.696 ns
G. Gokhale[6]	8-bit	1380	45.678 ns
G. Gokhale[7]	8-bit	1293	44.358 ns
Proposed Vedic Multiplier	8-bit	978	24.103 ns

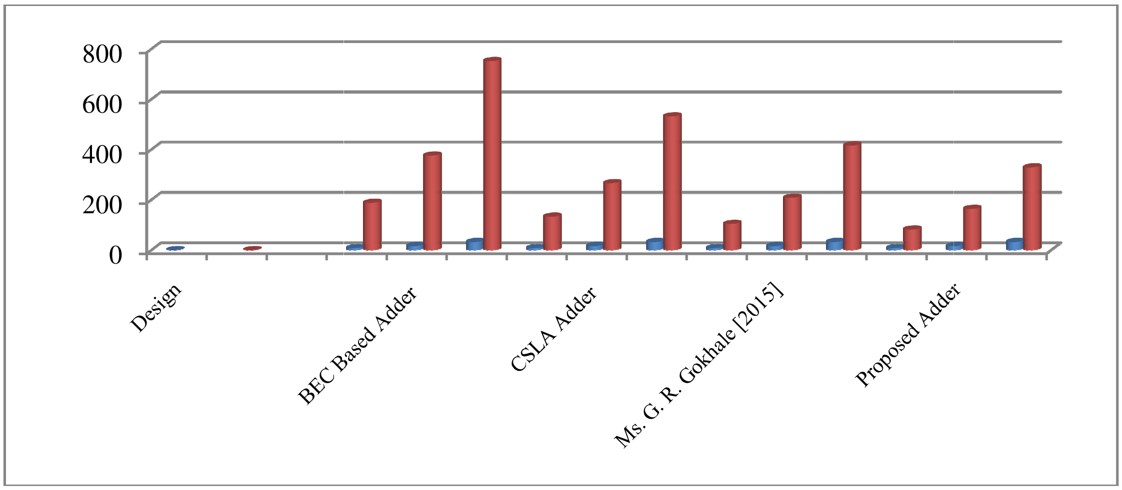

Figure-8: Bar Graph of the different types of adder.

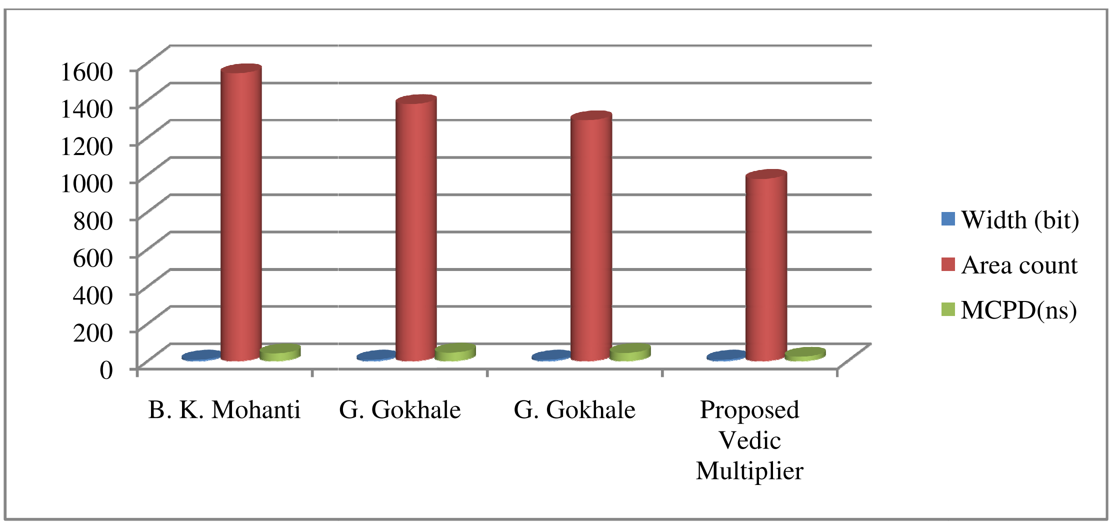

Figure-9: Bar Graph of the different Vedic Multiplier.

Table-3: Device utilization summary of 2-D DWT.

Design	Width	Area count	MCPD
Existing 2-D DWT	8-bit	17845	67.696 ns
Proposed 2-D DWT	8-bit	13253	51.943 ns

This DWT design has used image compression and due to Vedic multiplier it has give better result as conventional DWT and it is compared with Matlab image compression results. We have taken input image data using Matlab and DWT computation is synthesized in system generator and further quantization is done in Matlab. In the given design insert compression Factor between 1-100% as shown in below screen Figure-8. Input image having compression factor 50 and the input image is showing below Figure-10. When compression has been applied to this input image then new compressed image having compression factor 20% with PSNR shown in Figure-11.

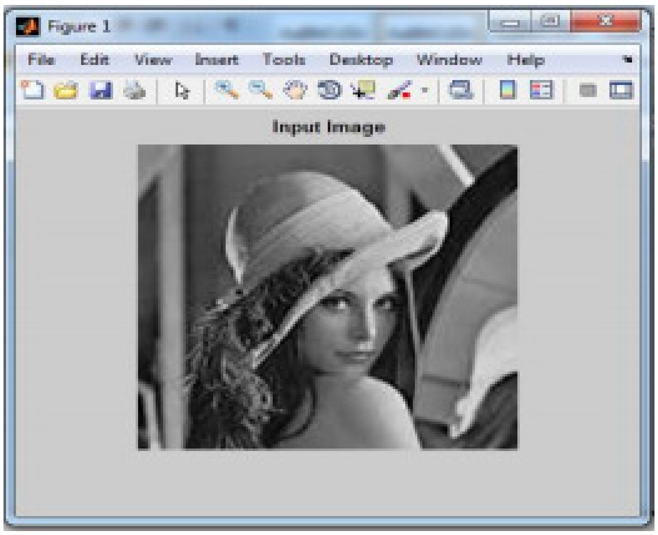

Figure-10: Input Image.

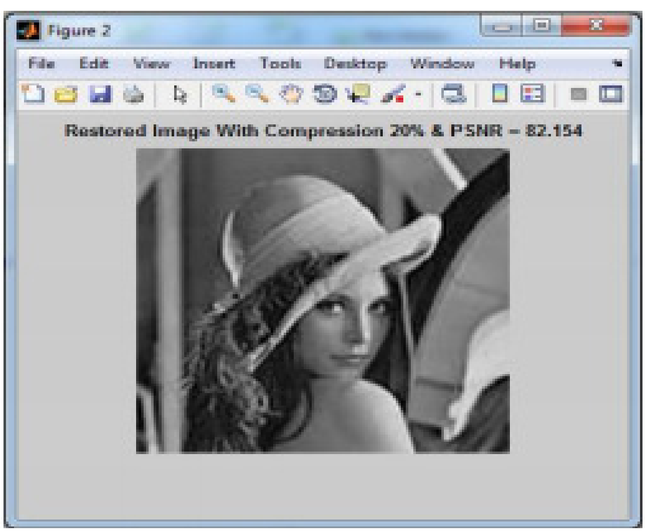

Figure-11: Compressed Image.

Conclusion

The proposed parallel and folded architectures are individually best amongst the existing structures. These designs have specific features like throughput scalability, memory efficiency, higher memory utilization efficiency and regular data flow. These features are very useful for hardware implement of 2-D DWT structure to meet area, speed and power requirement of different image processing applications. An effective architecture design for DWT computation based on the Vedic Mathematics on FPGA's for grey scale images. Standard test images are used to test functionality of design. Result shows increased speed of processing by the use of Vedic multiplier (Urdhava Tiryakbhyam). Proposed architecture is area and power efficient compared with other architectures, with high accuracy in terms of PSNR. However, proposed structures have few shortcomings like critical path delay, fixed point error, and interconnect delay which could be further investigated to reduce the area-delay-power of the 2-D DWT structures. These issues will be addressed in the future work.

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