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Review Paper

Signal Conditioning for Residential Power Monitoring Applications in the Electric Grid

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Abstract

This paper presents and analyzes analog front-end designs for the coupling of high-voltage and high-current bipolar signals to low voltage single supply analog to digital converters. The primary application is in the measurement of voltage, current, and power factor in single-phase residential power and energy meters that utilize microcontroller based architectures.

Keywords: Power monitoring, Energy meter.

Introduction

Historically, electrical energy monitoring for residential applications has measured kilowatt-hours via the revolving-disk watthour meter. In this technique, current and potential transformers are used to reduce the voltages and currents to a level appropriate for driving an electric motor; the rate of rotation of the motor shaft is proportional to the power flow in the circuit, and therefore energy usage over a defined time period is determined by taking the difference between two consecutive readings of the motor's shaft position[1]. Modern electric systems are increasingly abandoning electromechanical measurements in favor of digital devices, such as smart electric meters. Unlike traditional meters, smart meters measure the instantaneous value of the circuit's voltage and current, enabling a calculation of instantaneous power, reactive power, power factor, frequency, harmonic content, and energy[2]. One of the driving factors for the adoption of smart meter is the need for advanced metering infrastructure (AMI), in which the electricity meter is part of a two-way communication system between the local electric utility and the residential or industrial customer. AMI infrastructure enables electric utilities to gather instantaneous information about individual and system demand, as well as remotely control the meter to implement functions such as load management, service disconnection, or time-of-use pricing[3].

The deployment of smart meters to replace electromechanical meters is likely to continue to increase, as AMI is often considered a fundamental requirement, and therefore a first step, in electric grid modernization[4]. Additionally, power and energy monitoring applications using digital monitoring equipment are increasingly being included in devices and services inside of the customer's home, often with the goal of adaptive infrastructure and automation through technology. Examples include the Google Power Meter, an application program interface (API) designed to record residential electricity usage in near real-time and the kill-a-watt, an inline energy usage and cost monitor[5].

The increasing array of applications for digital electric meters has resulted in an increase in the need for low-cost and accurate digital integrated circuits (ICs) for metering. In general, two different solutions to the digital metering challenge exist: application specific multifunction metering ICs or general purpose microcontrollers. Both of these approaches typically utilize an on-chip analog to digital converter (ADC), an electronic circuit that converts the analog voltage and current input signals into a digital signal for data processing, computing, and communication. Typically, such system work on a 3.3, 5, or 10 volt range, and often have differential voltage inputs on the order of $\pm 500mV$, far less than standard 120 volt root-mean-square (RMS) amplitude of the U.S. residential power network. Therefore, a need exists for robust and cost efficient methods of signal conditioning such that the high voltage and current waveforms are converted to signal levels appropriate for use by an ADC. Specifically, the voltage waveform must be attenuated, the current waveform must be converted into a voltage waveform and the signals should be filtered to remove non-fundamental frequency components. This paper presents the design constraints for such systems and hardware circuits appropriate for the interfacing of high voltage and high current bi-polar signals with low voltage electronic devices.

Power Measurement Theory

Residential distribution voltage in the U.S. is supplied as a $120V_{RMS}$nominal cosine waveform and the resultant current waveform drawn by a load is also sinusoidal. Therefore, voltage and current are expressed as:

$$v(t) = V_m \cos(\omega t) \text{ (volts)} \quad (1)$$

$$i(t) = I_m \cos(\omega t + \theta) \text{ (amps)} \quad (2)$$

Where V_m and I_m are the peak current and voltage, ω is the angular frequency of the sinusoid, and θ is the phase shift between the voltage and current waveform caused by the impedance $Z = R \pm jX = |Z| \angle \theta$ of the load device. Power is the rate at which energy flows from the source to the load, and is the product of the instantaneous voltage and current waveforms:

$$p(t) = v(t) \text{ x } i(t) = V_m I_m \cos(\omega t) \cos(\omega t + \theta) \text{ (watts)} \quad (3)$$

Application of trigonometric identities results in the standard equation for instantaneous power:

$$p(t) = \frac{V_m I_m}{2} \cos(\theta) (1 + \cos(2\omega t)) + \frac{V_m I_m}{2} \sin(\theta) \sin(2\omega t) \quad (4)$$

The terms in Equation 4 can be rewritten as:

$$p(t) = P(1 + \cos(2\omega t)) + Q\sin(2\omega t) \quad (5)$$

The term containing the cosines is always positive and is the portion of the instantaneous power that is being delivered to the load. The term containing sines alternates between positive and negative, and is the portion of the instantaneous power that is being exchanged between the source and the inductive or capacitive portion of the load. Figure 1 illustrates instantaneous voltage, current, and power for two different current angles: $\theta = 0^0 and\ \theta = 45^0$. For the in-phase circuit, instantaneous power is always real, i.e. it is being delivered to a purely resistive load. In the lagging circuit, instantaneous power is both positive and negative, indicating that the circuit is extracting power from the source for a portion of the cycle, and then delivering power back to the source from the energy stored in the inductive load.

Figure-2 decomposes the instantaneous powers plotted in Figure-1 into the terms of Equation 5. For the purely resistive case, the sine function evaluates as 0, and the instantaneous power is purely positive. For the leading case, the resistive component consumes power, while the inductive component alternates between providing and extracting power from to/from the circuit. The consumed power in a circuit is always positive, and has an average value P, called the real power, measured in watts. The term Q is the maximum value of the pulsating power, and is called reactive power, measured in volt-ampere-reactive. Power measurements circuits must differentiate between P and Q in circuits for all applications: i.e. billing, control, and automation.

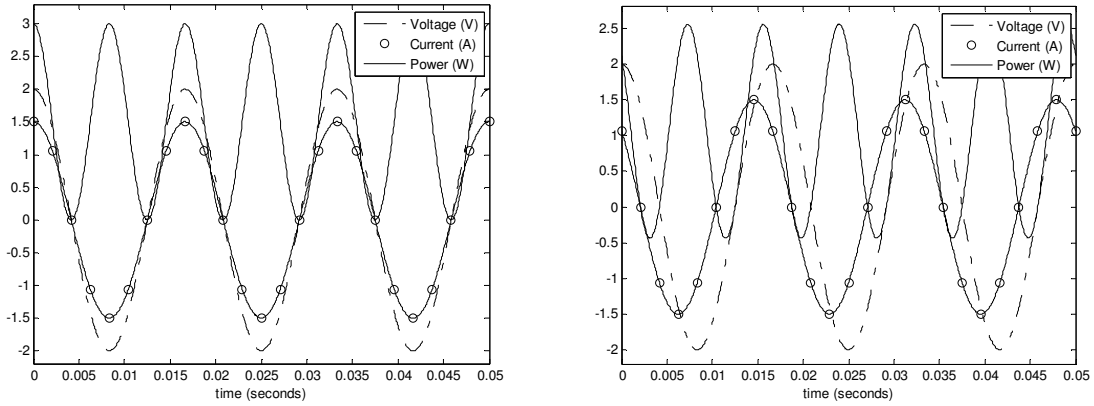

Figure-1
Instantaneous voltage, current and powr for in-phase (left) and lagging (right) circuits

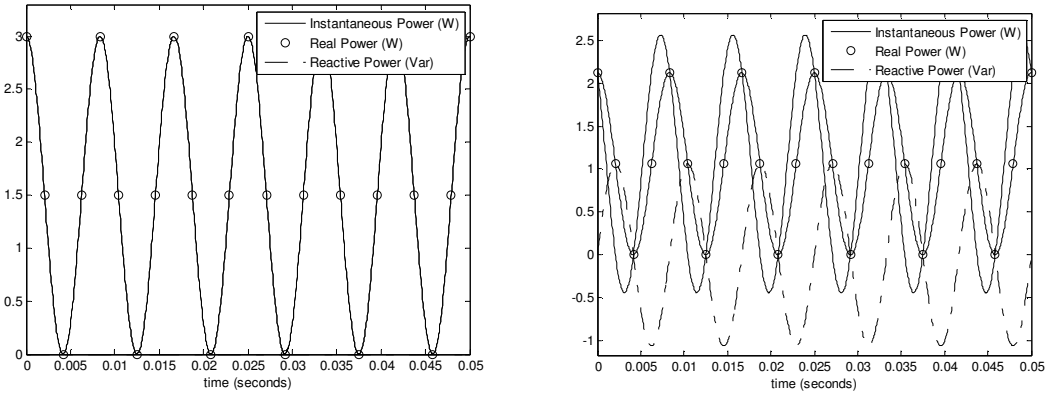

Figure-2
Instantaneous, real, and reactive power for in-phase (left) and lagging (right) circuits

Inspection of equations 4 and 5 reveal that P and Q can be generated by multiplication of the current and voltage signals only, which is performed via two different methods in electronic based measurement systems. In most IC based systems, instantaneous power is calculated by separating the current signal into an in-phase component and a quadrature component. Both signals are then multiplied in real-time by the voltage waveform, and P and Q can be extracted via low-pass filters. In a microcontroller measurement systems, i(t) and v(t) are sampled at discrete intervals. Their associated waveforms can then be reconstructed, and P and Q calculated directly from Equation 4.For both methods, it is important that the v(t) and i(t) signals accurately represent the voltage and current in the circuit. Any phase, gain, or offset error introduced by signal transducers will result in calculation errors in P and Q, with gain and offset errors effecting V_m and I_m, and phase errors effecting θ.

Measurement Error: The measurement of the voltage and current waveforms have error associated with them that stems from three sources; phase error between the voltage and current, and offset and gain/magnitude error of the individual channels. Measurement error is typically expressed as a percentage of the ideal or actual value:

$$\text{MeasurementError} = \frac{\text{MeasuredValue}-\text{ActualValue}}{\text{ActualValue}} \text{x } 100\% \quad (6)$$

Figure-3 shows the effects of these errors on a sinusoidal signal. Phase error manifests as a signal that is delayed in time with respect to the ideal signal. The phase error of 45 degrees has been exaggerated from typical values of up to 2 degrees in practical systems. Magnitude error is the difference between the measured amplitude of the analog input as compared to the ideal and has the effect of amplifying or attenuating the magnitude of the signal. Figure-3 shows a waveform that is attenuated by 25% of its ideal value. Offset error is the introduction of an external dc voltage and has the effect of increasing the average value of the waveform. Figure three shows a signal with an offset of 0.3 volts.

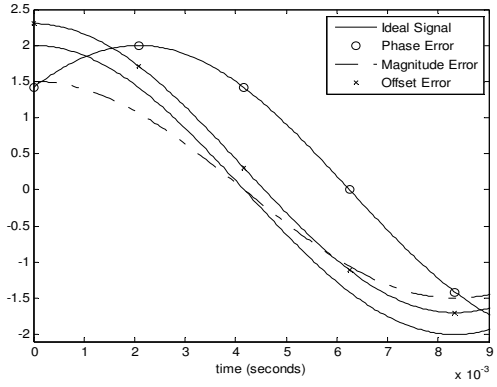

Figure-3
Classifications of error in sinusoidal current and voltag signals

Phase error is a result of two separate phenomenon in digitally sampled systems: phase shift introduced by the external sensor caused by inductive or capacitive effects of the signal conditioning circuit (i.e. lag and lead), and phase delay introduced by the sampling algorithm caused by non-simultaneous sampling of the v(t) and i(t) waveforms. Typically phase error is not rectified in the signal conditioning system. Instead, it is most often compensated for by a time-delay calibration algorithm executed by the IC or microcontroller. Offset error occurs when a dc offset voltage is introduced from an external source into the analog inputand can be compensated for in signal conditioning hardware design by including a high-pass filter into the analog input channel of the ADC. More commonly, the DC component is removed by using a digital high-pass filter of the Infinite Impulse Response (IIR) type. Magnitude error occurs to due component tolerances in the design of signal conditioning circuits involving amplifiers, attenuators, and buffers. It can be rectified either through hardware tuning of components in the signal conditioning circuit (typically adjusting a potentiometer), or, more commonly, can be calibrated for in a software routine.

Analog-to-Digital Converter Requirements

Unlike their electromechanical counterparts, smart meters contain solid state analog to digital conversion devices to convert the voltage and current waveforms into digital signals, typically utilizing a high-resolution ADC for both the voltage and current inputs[6]. Most often, the analog voltage and current signals of interest cannot be directly connected to the inputs of the ADC. Instead, they must be undergo a signal conditioning process to make them compatible with the input requirements of the circuit. Therefore, the input signal requirements of the ADC analog input channels are the primary driver of the signal conditioning circuit output specifications. Typically these are input type, input polarity, and input range[7].

Generally, ADCs can either accept single-ended or differential inputs. Single ended inputs are all referenced to a common ground, and therefore each channel of the ADC requires only a single input pin. The analog ground pin used as a reference is shared between all input channels. Differential inputs require two analog input to the ADC, and the ADC digitizes the difference between the two signals.

The majority of ADC can only accept positive voltages as analog inputs. Such devices have a minimum input voltage of 0V and are referred to as unipolar devices. In contrast, bipolar ADCs can accept both positive and negative input voltages.

ADCs utilize an internal reference voltage (V_{ref}) to perform digitization; analog input signals are converting into a binary number that represents the ratio of the analog input to the reference. Often, the reference voltage of an ADC is configurable in software, however input voltage must always be less than the reference voltage, or saturation will occur. The

input range of the ADC is determined by combing the polarity information with the reference voltage, for example 0 to $+V_{ref}$ for a unipolar device or $-V_{ref}$ to $+ V_{ref}$ for a bipolar ADC.

Hardware Design Case Study

This section demonstrates hardware design of a signal conditioning circuit based on a residential single phase power monitoring application using the Arduino UNO, a microcontroller board that utilizes the ATmega328P microcontroller from Atmel.

Signal Requirements: U.S. Residential Distribution Loads: Electric power delivery to residential loads in the U.S. is governed by the American National Standard for Electric Power Systems and Equipment – Voltage Ratings (60 Hz)[8]. This standard defines the nominal distribution voltage as 120VRMS with an acceptable utilization range of $110V_{RMS}$ to $125V_{RMS}$ (i.e. Range A). However, excursions beyond this range occur from 106V to 127V (i.e. Range B). Typically current loads are up to 12A on a 15A circuit or 15 A on a 20A circuit; for example, a 1400 W microwave oven will draw approximately 12A of current while a small LCD television may draw only 0.5A.

ADC Requirements: The ADC module of the ATmega328P converts a single ended analog input voltage to a 10-bit digital number between GND and V_{ref} (i.e. single ended input range of 0 to $+V_{ref}$)[8]. The reference voltage of the ADC is software programmable to either 1.1V or an external reference pin. The Arduino UNO used in this case study is configured to use a 5V external reference for an analog voltage input range of 0 to +5V.

Hardware Design: An analog front end circuit is used to convert the high voltages and currents of the load to a voltage level sufficient for direct measurement by the ADC of the ATmega328P; i.e. $5V_{pp}$ with a DC offset of 2.5V. As such, the voltage input must be attenuated and level-shifted, the current input must be converted to a voltage, amplified, and given a DC bias. Additionally, an anti-aliasing low-pass filter is included to eliminate frequency components of the voltage signal higher than half of the ADC sampling rate.

Voltage Front End: To accurately measure residential power, the measurement system must be capable of transducing a voltage signal v(t) up to $127V_{RMS}$ ($179.6V_P$) and as low as $106V_{RMS}$ ($149.9ZV_P$). Therefore, these high-voltage signals must be converted to levels appropriate for the ATmega328P ADC using a voltage front end circuit. These tasks can be achieved using the attenuator and level shifter shown in Figure-4.

The resistor ladder R1-R2 is used as a voltage divider to reduce the input voltage waveform to a $5V_{pp}$ signal when the supply voltage reaches 127 V_{RMS}, the maximum value of ANSI C84.1 Range B:

$$V_{div} = V_{source} X \frac{R_2}{R_1+R_2} \quad (7)$$

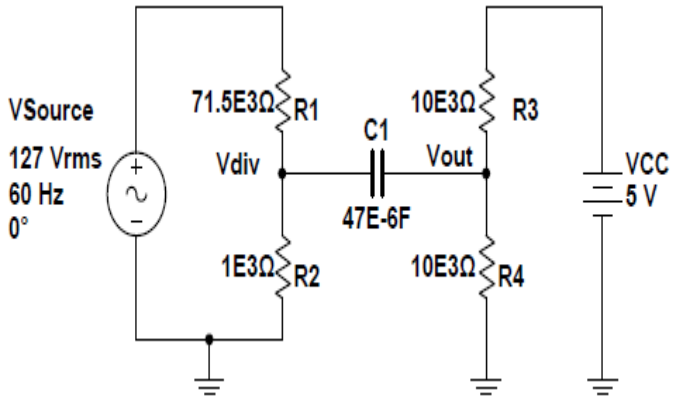

Figure-4
Voltage front-end circuit

Application of Formula 7 results in a voltage divider ratio of 71.842:1. Choosing the nearest standard value 1% resistors as 1kΩ for R_2 and 71.5kΩ for R_1 results in a division ratio of 1:72.5005. The output voltage under the voltage boundary condition is then:

$$V_{div} = 127 \cdot \sqrt{2} \cdot \frac{1k}{71.5k+1k} = 4.95462\ V_{PP} \quad (8)$$

This signal is then AC coupled through series capacitor C1 into a DC bias ladder formed by the R3 and R4 ladder:

$$V_{DC} = V_{CC}\, X \frac{R_4}{R_3+R_4} \quad (9)$$

The filter capacitor C1 removes the DC component from the signal, which centers the AC signal at 0 volts. For the ATmega328P, a 2.5 volt offset can be delivered by a 5V DC supply by using matched resistors:

$$V_{DC} = 5\ X \frac{10k}{10k+10k} = 2.5V \quad (10)$$

In most DAQ applications, the voltage input will be provided to a multiplexed ADC input. This design configuration presents an additional challenge: the voltage divider appears as a lower impedance source than a direct analog input and the output impedance of the divider is too high for most multiplex inputs. Addition of an analog buffer of unity-gain to the divider output overcomes these problems; the buffer presents a high impedance to the source and a low impedance to the multiplexed analog input of the ADC[10].

Since ADCs typically operate on a single supply, the buffer circuit should be combined with offset circuit of Figure-4 using a summing amplifier. A similar buffer can be added to the voltage offset circuit, as shown in Figure-5.

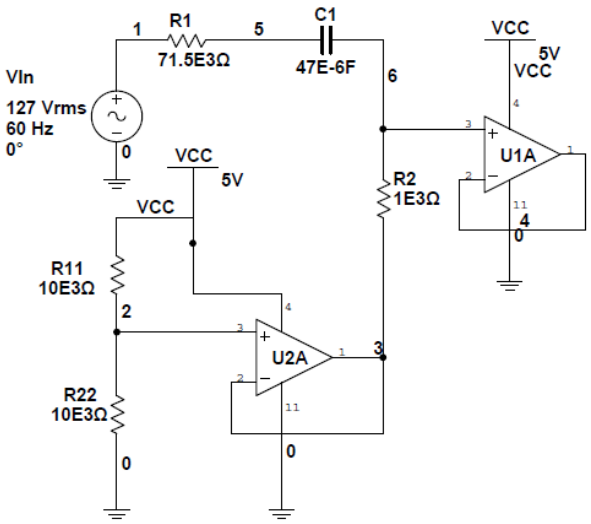

Figure-5
Voltage front-end circuit with attnuator and level-shifter

In this configuration, the output voltage of the summer (V_{out}) at peak voltage is:

$$V_{out} = V_{In}\frac{R_2}{R_1+R_2} + V_{CC}\frac{R_{22}}{R_{12}+R_{22}} = 127\sqrt{2}\frac{1E3}{71.5E3+1E3} + 5\frac{10E3}{10E3+10E3} = 4.977V \quad (11)$$

Current Front End*:* A current front end is included to convert the current signals to voltages in the acceptable range of the ADC. Because the current varies over a large range (0A to 15A), measurement accuracy of this section is a major design consideration. The current of the load is converted to a lower value using a current output type current transformer (CT). The current output can be converted to a voltage output by driving a burden resistor. The value of the burden resistor is calculated by calculating the peak current in the secondary coil. For residential energy application in the U.S., a value of $20A_{RMS}$ is chosen as peak. This application uses a CT with a turn ratio of 200A:26.6mA. The burden resistance (R_B) is therefore:

$$R_B = \frac{\frac{V_{Ref}}{2}}{I_s} = \frac{\frac{V_{Ref}}{2}}{I_P(\frac{I_2}{I_1})} = \frac{\frac{5}{2}}{20\sqrt{2}(\frac{26.6E-3}{200})} = 665\Omega \quad (12)$$

From this value, the min and max output voltage of the CT under load are found from:

$$V_{out} = I_{Load}\left(\frac{26.6E-3}{200}\right)(665) \quad (13)$$

Using $20A_{RMS}$ as $I_{Load\ Max}$ and $10mA_{RMS}$ as $I_{LoadMin}$ results in an output voltage range of .002502 to 5 V_{PP}. The resolution of an ADC is given by:

$$V_{Res} = \frac{V_{Ref}}{2^{n-1}} \quad (14)$$

Where V_{Ref} is the full scale operating voltage of the ADC and n is the number of bits of the ADC. The ATmega328P utilizes a 10-bit ADC with a full scale voltage range of 5V. V_{Res} is therefore 9.76563 mV, which is too large to measure $I_{LoadMin}$. To achieve 1% or better measurement accuracy over this wide current range requires that the measurement circuit employ a gain change in the amplification stage[11]. This can be achieved by implementing multiple amplifiers with different gain values, or by dynamically adjusting amplifier gain by changing the feedback resistor.

To measure the .002502V_{PP} output of the current transformer to 1% accuracy, the ADC must be able to resolve down to 25.02μV_{PP}. Therefore the voltage amplifier must provide a gain A_v=391. Table-1 summarizes the different gain stages necessary to achieve the necessary voltage/current resolution across the full scale measurement range.

Table-1
Gain stage settings for current front end amplifiers

Amplifier Gain (Av)	Current Resolution (A_{pp})	Min Current (A_{RMS})	Max Current (A_{RMS})
391	282.8u	10m	51.1m
76	1.45m	51.1m	25.57m
15	7.34m	259.57m	1.25
3	35.33m	1.25	5
1	141.33m	5.00	19.99

Unlike the attenuating voltage front-end, the current front-end must simultaneously amplify and offset the input voltage from the current transformer circuit. A common strategy is to use an inverting amplifier topology and to apply a voltage offset to the non-inverting input of the amplifier[12]. The inverted current data can then be inverted in software. Figure-6 presents an implementation of the gain stages from Table-1. The different gain stages can either be selected by using digitally controllable switches, or by implementing a piecewise linear amplifier.

Test Results

Figure-7 shows the time-domain voltage amplifier response to a 127VRMS input signal, corresponding to the maximum input distribution voltage signal. The level shifting circuit produces the required offset voltage, and the attenuation/level-shifting circuit creates the $5V_{PP}$ waveform with 2.5VDC offset necessary for the ATmega328P. Since the input signal is ac coupled through the input capacitor, and DC offset from the original signal is filtered.

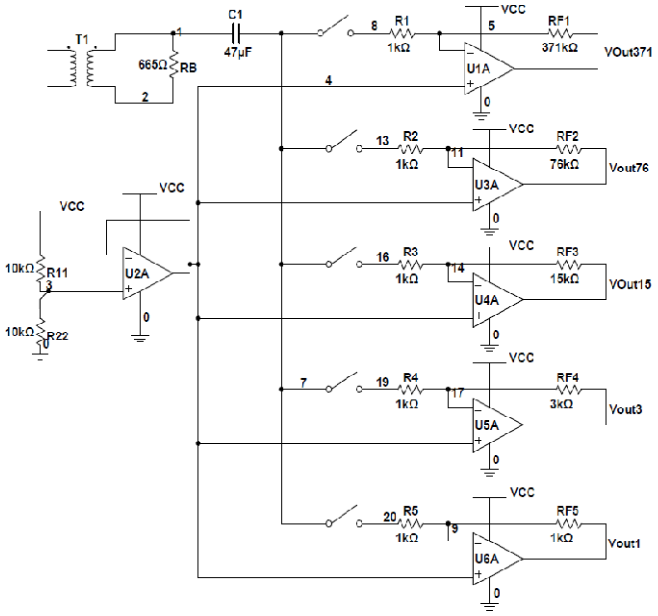

Figure-6
Current front-end circuit with variable amplification and level-shifter

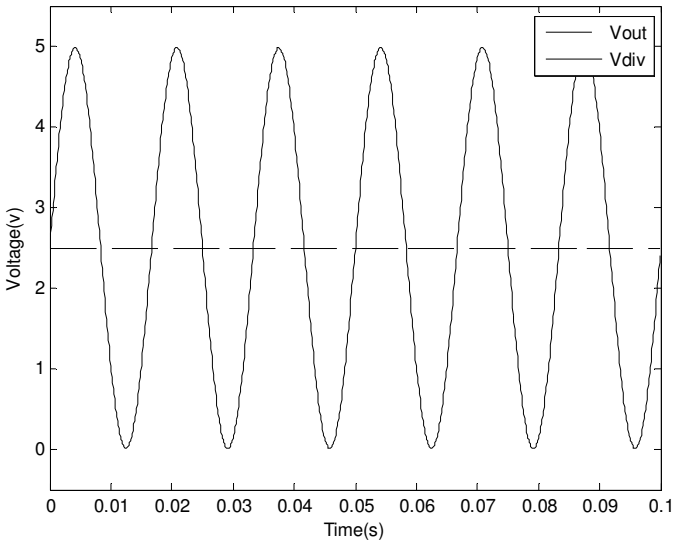

Figure-7
Output voltage signal for voltage front end in response to 127VRMS input

Figure-8 presents a Bode plot frequency response graph for the output voltage magnitude and phase shift for the voltage front-end circuit. At 60Hz, the circuit responds with -37dBV of attenuation, while introducing a phase shift of 0.04Hz, well within 1% accuracy. The circuit begins to see voltage attenuation of unacceptable levels above 10 MHZ, and unacceptable levels of phase shift above 1MHz. however, these values are far above the fundamental, as well as the commonly metered harmonics 2-11.

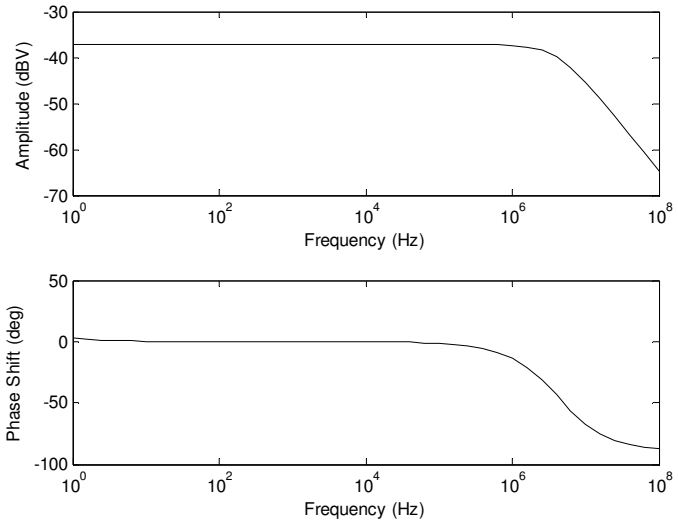

Figure-8
Bode plot of voltage front end

Figure-9 presents the output voltage signal for the current front-end in response to a load current of 0.8 A_{RMS}. According to Table-1, 0.8 A_{RMS} is most accurately measured by the A_V=15 amplifier. As shown in Figure-8, A_V= 371 and A_V=76 both saturate at the supply to the op-amp. While the remaining circuit (A_V=15, A_V=3, and A_V=1) amplify, the A_V=15 circuit creates a ~3V_{PP} out signal with a 2.5V_{DC} offset, providing the greatest current resolution.

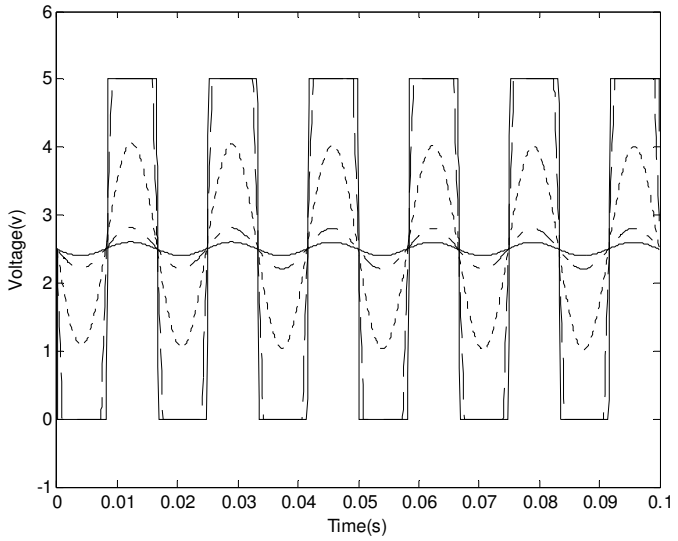

Figure-9
Output voltage signal for current front end in response 200mVpp (0.8ARMS) input

Figure-10 presents a Bode plot frequency response graph for the output voltage magnitude and phase shift for the current front-end circuit. The gain of the amplifier at 60Hz is 51.8, 37.6, 23.5, 9.5, and 0 dBV for A_V= 371, 76. 15, 3 and 1, respectively. Additionally, the circuit introduce a phase shift of -177.3 for AV=371, and -177.0 for all other gain settings.

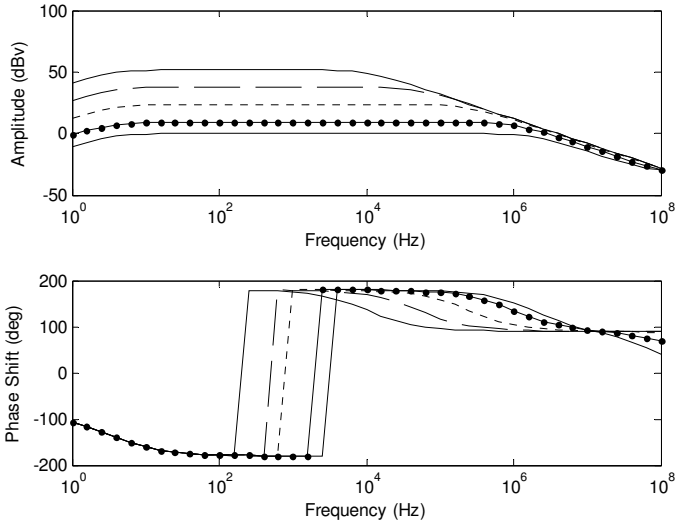

Figure-10
Bode plot for current front-end

Conclusion

This paper has presented op-amp based voltage and current converters to interface low-voltage single supply microcontroller-based analog to digital converters to the residential distribution system for power and energy monitoring applications. The voltage font-end blocks DC, attenuates the supply voltage and adds a DC offset compatible to the ADC. The current front-end is composed of a gain-selectable inverting amplifier and a DC offset circuit. The gain-selection is included to allow 1% or better measurement accuracy across a current range from 10mA to $15A_{RMS}$. Frequency analysis of these circuits shows them to be gain stable across all frequencies of interest, in particular over the first 11 harmonics of input waveforms. Although not the focus of this paper, such capability is important for power quality analysis of the voltage and current waveforms.

The circuits presented in this paper are suitable as the signal-conditioning interfaces for low-cost energy and power meters. Applications such as energy management, low cost metering, and plug-load monitoring can be more cost effectively realized utilizing the presented architectures.

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