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Resolution, Range and Area Comparison of Digital CMOS Time to Digital Converter Techniques

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Abstract

This paper demonstrates the comparison of various (TDC) Time to Digital Converter, on the basis of Resolution, Range and Area. Digital TDC is used as direct measurement of time interval between two skew signals. In digital PLL it is used as a phase detector.TDC also have applications in the field of Measurement and Instrumentation such as digital scopes, in wireless applications such as digital frequency synthesizers and for time of flight measurement. Observation is shown for (BDL) Buffer delay line based TDC,(IDL) Inverter chain based TDC and (VDL) Vernier Delay Line based TDC. Various TDC circuits having 32 stages were implemented using 28nm FDSOI CMOS technology and we have compared its results on the basis of Resolution, Range and Area. Analysis of resolution variation with respect to the Power supply and Temperature variations has been done.

Keywords: Resolution, dynamic range, TDC, buffer delay line, inverter delay line, VDL.

Introduction

As technology shrinking towards the picoseconds range, the precise measurement of the time interval between two events is needed. Previously used method based on ADC (Analog Data Converter) for time measurement is not efficient due to low resolution andaccuracy limitations. In recent technology node, very fine timing resolution is a common challenge.TDC is primarily used for precise time skew measurement between two skewed signals. Analog TDC's are based on current integration, while the digital TDCs are based on some counting methods. Various Digital methods are used for fine time interval measurement and are known as digital TDC. TDC has been used in various applications such as in instrumentation, time-of-flight measurement, digital phase-locked loops (PLL), in High speed signal capturing andhigh-energy particle physics and demodulators. In this paper buffer delay line based, inverter delay-line based and Vernier delay line based TDCs are analyzed. Comparison of their resolution and range for 28nm FDSOI technology is presented. Resolution is defined as the minimum value that can be measured. Range is defined as the maximum skew between two signals that can be measured.

The paper is arranged as follows. In Section II, the background of time measurement system and its limitation is being explained. In Section III, the basic principle for measuring precise time between two signals is presented. BDL-TDC, IDL-TDC and VDL-TDC is implemented in Section IV. In section V experimental results are shown, Section VII concludes the paper.

Background

Traditionally the analog approach is used for time measurement between two signals, which first convert the information of time domain into the analog voltage and after that, this analog voltage is converted into the digital domain through conventional ADC. However this approach degrades the performance of TDC in terms of resolution, this approach is termed as first generation. While in another approach, fully digital method is used for time measurement where no need to convert time into voltage, i.e. there is a direct conversion of time domain into digital domain. Due to reduction of conversion step, resolution is improved and implementation become simpler than first generation, this approach is called as Second Generation[1].

A paradigm is defined in the time to digital conversion as *"In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals"*[2].

Previously counter is used in digital time interval measurement. In counter based time measurement, time is quantized by the time period of reference clock cycle i.e. Tclk. In figure-1, Signal_A and Signal_B are two skewed signals which are fed to the Pulsegen block which generates pulse. The output of the pulsegen along with the Reference clock is fed to the counter's clock. Time interval is determined by the output of counter value multiply by its reference clock period.

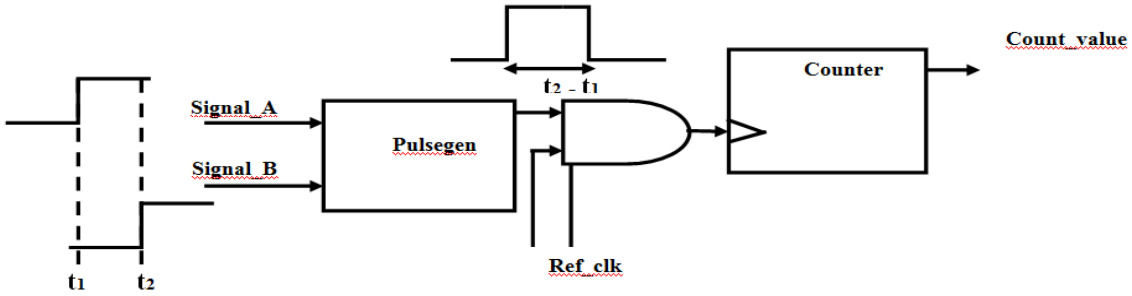


Figure-1

Two signals A and B are completely asynchronous to reference clock as shown in figure- 2, causes high error in measurement i.e. low resolution which limits the use of counter for time measurement, while it has a high or unlimited dynamic range[1]. The measurement time interval Δ T can be expressed as

Δ T=n * Tclk

The resolution (quantization error) of the ΔT measurement is limited to two fold the period of the reference clock signal. (For e.g., for 200 MHz frequency, resolution is 10ns) which is not suitable for precise time skew measurement.

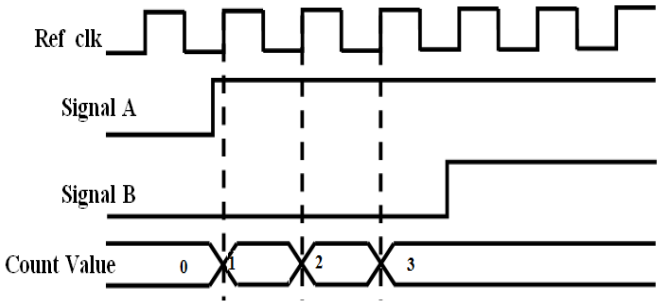


Figure-2

Principle of TDC

As we are moving in deep submicron technology, high resolution is required for precise time measurement. Resolution is increased by increasing the clock frequency, however this increase the power. In addition it is very difficult to provide stability in high frequency and higher frequency means less time, so counter may not be able to increase the count due to very less time (for e.g., for 1Ghz frequency, time period or resolution is 1ns). So, increasing frequency to increase resolution is not an efficient approach.

A higher resolution is achieved by subdividing one clock period into many small time intervals as shown in figure- 3. Divide the Reference clock period by r subinterval i.e. increase the resolution by factor r where r is called as interpolation factor.Clock Cycle Interpolation approach increases resolution by factor r.

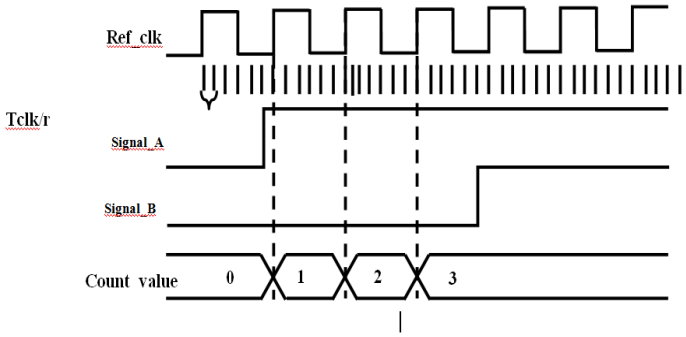


Figure-3

Implementation

Buffer Delay Line based TDC: 32 stage Buffer Delay Line based TDC is implemented using 28nm FDSOI technology process. This contains number of buffers with well-defined delay timet_d of each buffer; these buffers are connected as chain. Output of each buffer goes to Flip Flops (FF), these FFs output is goes to Thermometer code detector as shown in figure-4. Signal_A and Signal_B are two skewed signal which is applied to first input buffer and CLK input of all FFs respectively. Signal_A is propagated along the delay line which is delayed by the delay of buffer, as output of buffers goes to FF so that FF changes its output, if it does so, it considered as transparent. When Signal_B signal arrives, Signal_A cannot propagate further and state of FF is sampled parallel. FF output is HIGH where Signal_A is passed, otherwise it is LOW

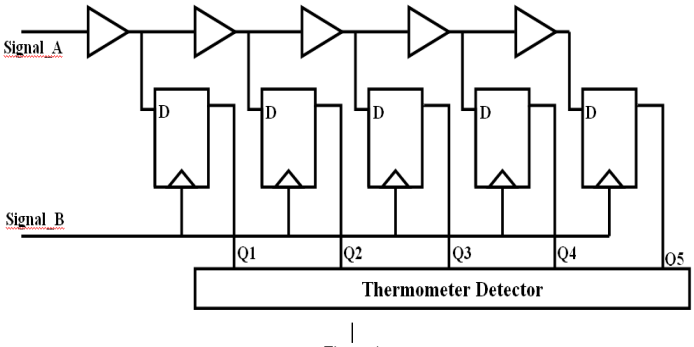


Figure-4

Time interval between Signal_A andSignal_B is proportional to number of FF that are HIGH, which is detected by thermometer code detector i.e.by HIGH to LOW transition[1,2]. The resolution of the buffer delay-line based TDC is limited by the delay of the buffers. It cover dynamic range of n*t_d where n is number of stages.

Inverter based TDC*:* 32 stage Inverter based TDC is implemented using 28 nm FDSOI technology process. CMOS Inverter is used instead of buffers in buffer delay line TDC to increase resolution. FFs are used for sampling[6]. Output of FFs goes to Pseudo-thermometer code detector as shown in figure- 5. Here, Time interval between Signal_A and Signal_B is measured by phase change of the consecutive one-zero pattern, rather than by the number of transparent FFs[1, 2.]

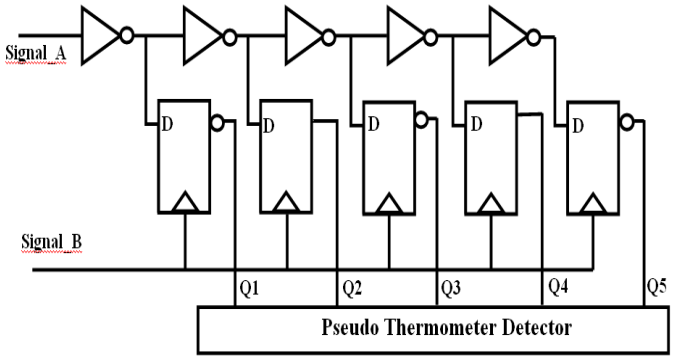


Figure-5

Since the resolution of the Inverter based TDC is doubled than buffer based TDC. Its dynamic range is n *$t_{inv}$where $t_{inv}$is delay of an inverter. Inverter increases the nonlinearity due to different Rise and fall transition which arise during ion implantation steps of manufacturing. Double chain of inverter can be introduced to compensate the abnormality of inverter[1]. This increases the complexity of an actual TDC implementation.

Vernier Delay Line based TDC: 32 stage Vernier Delay Line based TDC is implemented using 28nm FDSOI technology, combine the above two design concept such that two chain of buffer delay line is used having slightly different delay timest$_1$andt$_2$such that $t_1 > t_2$. Delay line 1 is belongs to Signal_A, while delay line 2 is affiliated to Signal_B. Output of buffer in delay line 1 and delay line 2 is goes to input D and input clk of FF respectively. This setting is named as Vernier Delay line or VDL as shown in figure- 6. Its operation is based on Nutt method[3, 4, 5].

During propagation, Signal_A is delayed by t_1 through one cell; corresponding FF state is considered as transparent. Signal_B is also propagating through delay line 2,which is delayed by t_2 through one cell, the difference between Signal_A and Signal_B is continuously decreases during propagation because $t_1 > t_2$. The difference between two propagation delay values gives resolution of VDL i.e. $(t_1 - t_2)$. Here, VDL having dynamic range of n *$(t_1 - t_2)$[3, 4 and 5].

Experiment Results

Various TDCs are implemented using 28nm FDSOI technology which consists of 32 stages. Result is shown in table- 1for typical process, 25C temperature and 1.8V voltage, having with fixed slope of 0.5ps.

Analysis is done by varying 10% of power supply and temperature from -20ºC to 135ºC. Its variation of resolution has been plotted which is shown in figure- 7, dependence of delay in both parameters change the resolution. By varying power supply, BDL, IDL, VDL give ± 2%, ±0.4%, and ±3% deviation of resolution respectively. By varying Temperature BDL, IDL, VDL give ±1.5%, ±1.5%, and ±4% deviation in resolution respectively.

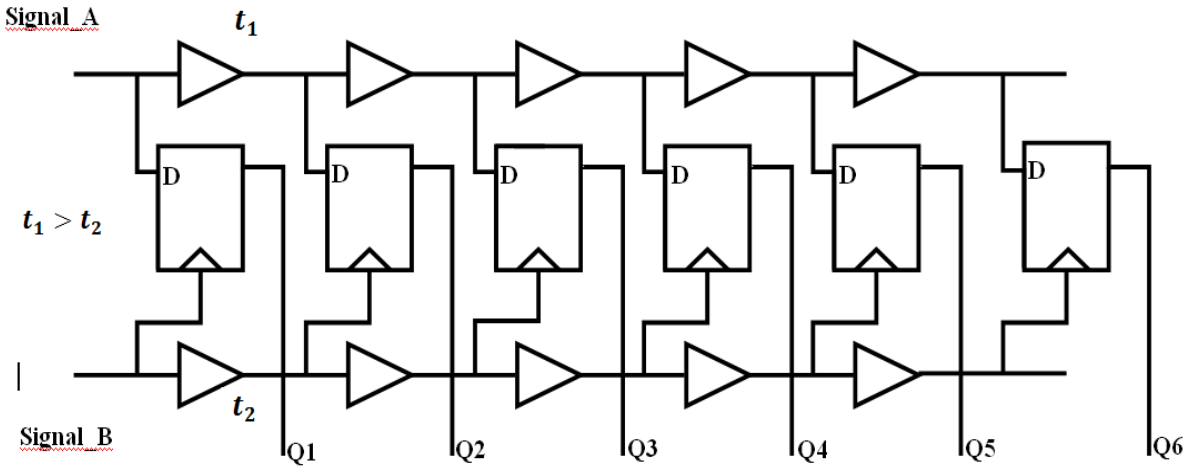
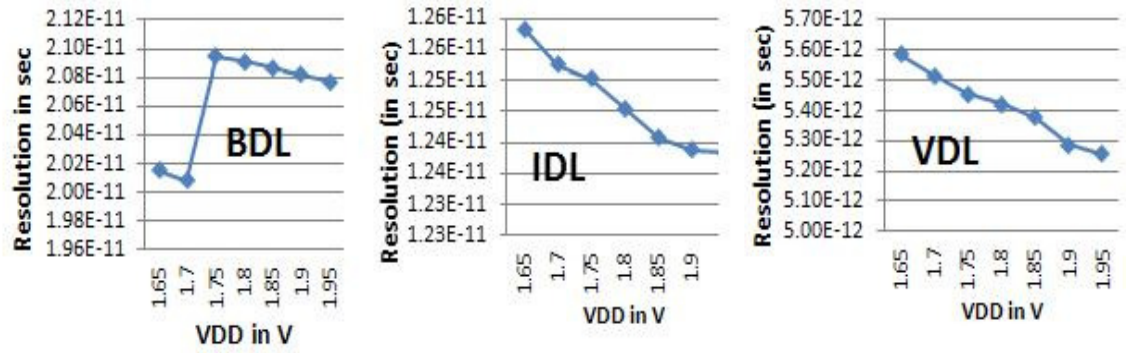


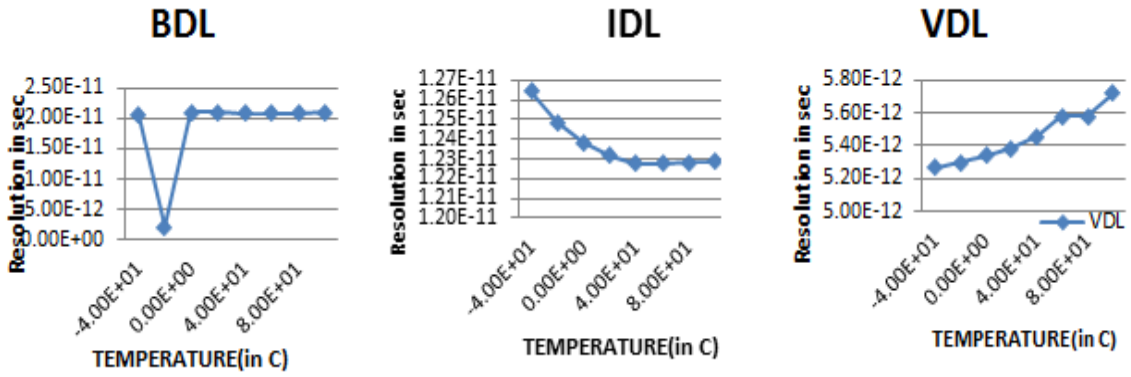
Figure-6

Table-1
Comparison result for 32 stages TDC techniques at Vdd=1.8v, Temperature=25ºCandInput slope=0.5p

TDC Technique	Resolution in(ps)	Dynamic Range in(ps)	Estimated Area using FDSOI 28 nm in (um²)
Buffer delay line based	21	672	215
Inverter delay line based	12	384	228
Vernier Delay line based	5	160	280



(a)



(b)

Figure-7

Conclusion

Various digital TDCs has been studied and analyzed. We observed that among all, VDL gives High resolution, but for less dynamic range. However BDL gives wide dynamic range but for less resolution, on the other hand inverter delay line based TDC give more resolution for less dynamic range as buffer delay line TDC, Also it increase nonlinearity due to different fall and rise delay of inverter. So, among all VDL is more efficient approach for precise time skew measurement though it takes more area. To increase its dynamic range, increasing number of stage is not appropriate method. Its range can be increased by introducing a counter or some other circuits which work as a coarse measurement and VDL approach is used for fine measurement.

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