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Evaluation of power MOSFET IRF150 using OrCAD capture

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Abstract

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a type of Field Effect Transistor, which acts as a voltage-controlled current device. It operates by controlling the width of the channel that lies between drain and source terminal. Depending upon the width of the channel along which the charge flows the operating region of the transistor is defined. These operating regions are cut region, triode region and saturation region. This paper presents the analysis and evaluation of IRF150 n-channel E-MOSFET in OrCAD Capture. The analysis includes the characteristics curve, voltage transfer function and power consumption of MOSFET. The evaluations of the small signal characteristics, analog and digital frequency response and maximum frequency of the MOSFET are also presented. Through the evaluation, the minimum threshold voltage required to turn on the transistor IRF150 is found to be 3V. The MOSFET exhibits switching logic threshold voltage of 2.872V. The resulting low noise margin and high noise margin are approximately +11.928% and -16.316% respectively. The power consumed with low input voltage is 126.020 nW and24.992mW for high input voltage. With the corner frequency of 55.857 KHz and slope of 18.975 dB/Decade the evaluated MOSFET circuit behaves like a low pass filter.

Keywords: MOSFET, OrCAD Capture, IRF150, noise margin, inverter, power consumption.

Introduction

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a unipolar transistor that acts as a voltage-controlled current device. The effects of an electric field control the flow of current; it acts as a switch and a signal amplifier. It is the key component in high frequency, high efficiency switching applications across the electronics industry[1]. The requirement of voltage in MOSFET has relaxed the driving requirement making it much simpler as compared to BJT (Bipolar Junction Transistor). MOSFET comes in two polarities, n channel MOSFET and p channel MOSFET. N channel MOSFET is more advantageous than p channel MOSFET as it has high packing density[2]. MOSFET can be either enhancement-mode (E-MOSFET) or depletion-mode (D-MOSFET) devices. E-MOSFET is normally off, turns on with a voltage, whereas D-MOSFET is normally on, and turns off with a voltage[3]. MOSFET has four-terminals: source(S), gate (G), drain (D) and body (B) terminal. The body of the MOSFET is frequently connected to the source terminal so making it a three-terminal device like field effect transistor (FET). In case of the n-MOSFET, the substrate is lightly doped (small number of holes) and the source/drain is heavily doped (large number of electrons).

Special type of MOSFET specially designed to handle high-level powers are known as Power MOSFET. Though the operating principle of power MOSFET is similar to the general MOSFET, it exhibits low gate drive power, fast switching speed and superior paralleling capability[4]. Compared to normal MOSFET, power MOSFET possess thick gate oxide with high threshold voltage and can withstand high input voltage.

Though there are various types of power MOSFET with different internal geometry, all of them are voltage-driven rather than current driven unlike BJT's. IRF150[5] is an N-Channel enhancement modesilicongate power FET. It is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. The paper presents the characteristics evaluation of IRF150 power MOSFET using OrCAD Capture[6]. The paper further evaluates the simulation of small signal characteristics and its digital frequency response.

Evaluation of IRF150 MOSFET characteristics

V-I Characteristics: IRF150 from EVAL library in OrCAD capture is used for its evaluation. The model has a bias value power of 8.333mW with PSpice model implementation type. The circuit diagram to evaluate its VI characteristics is shown in Figure-1. V_Vd rain, the drain voltage is swept from 0-5 V to achieve the characteristics. Its corresponding characteristics is shown in Figure-2.

From the Figure-2, until V_{GS} (gate source voltage) is 3V, the drain current (I_D) is observed to be zero. Small amount of current started to flow while increasing the V_{GS} slowly until 3V. This is identified as a turn-on point, the noted threshold voltage (V_{TH}) is 3V. The minimum voltage required by the transistor to turn ON is called threshold voltage[7]. Increasing the V_{GS} beyond this the current tend to increase with I_D=2.0808A at V_{GS}=4V and 7.1657A at V_{GS}=5V. It is observed that the I_D current and V_{DS} holds almost a linear relation until it reaches the pinch off voltage.

This region is called Triode region or Ohmic region. Pinch off voltage is the drain to source voltage after which the drain to source current becomes almost constant and the MOSFET enters into saturation region[2].

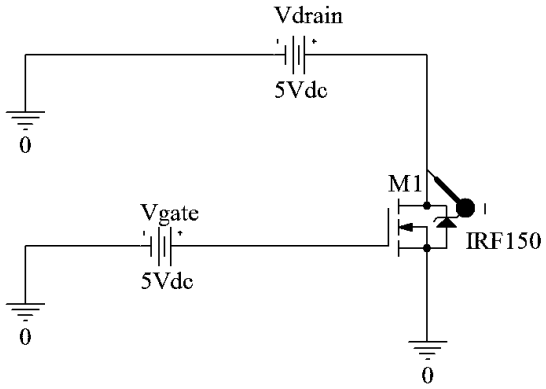

Figure-1: Simulation Circuit.

In Figure-2 for V_{GS}=5V, the pinch off voltage $V_{DS\ (pinch\ off)}$ is observed as 2.1564 V. Similarly, for V_{GS}=4V, $V_{DS\ (pinch\ off)}$ = 1.0859 V.

Voltage transfer function (VTF), power consumption and small signal parameters: A resistor of 1 kΩ and capacitor of 1pF is added to the circuit diagram of Figure-1 to evaluate its voltage transfer function[8] (V_{out} vs. V_{in}). As shown in Figure-3 the resistor is added between Vdrain and drain terminal and the capacitor as load capacitor. Using the achieved voltage transfer function, the noise margin[9] is evaluated by plotting the derivative at slope is equal to -1, as shown in Figure-5 and 6.

In the Figure-4, intersection of the straight line (drawn from (0,0) to (4,4)) with the VTF graph of V(Vout) of MOSFET is the logic threshold. The threshold voltage is the point where the input voltage Vgate is equal to the output voltage, Vout. From the graph the switching point or logic threshold is (2.8682V, 2.8682V).

From the Figure-6: Minimum HIGH input voltage, V_{IH} =2.8965V; Maximum LOW input voltage, V_{IL}=2.8311V; Minimum HIGH output voltage, V_{OH}=4.9886V; Maximum LOW output voltage, V_{OL}=0.032902V;

The noise margins of the MOSFET is: NML (Noise Margin Low) = ($V_{IL} - V_{OL}$) =2.8311-0.032902=2.7982V; NMH (Noise Margin High) = ($V_{OH} - V_{IH}$) =4.9886-2.8965=2.0921V; For an Ideal Inverter: NML = (VDD/2 – 0) = 2.5 V; NMH = (VDD – VDD/2) = 2.5 V;

Comparing NM with the ideal inverter[10]: For Noise Margin Low: (2.7982-2.5) / 2.5=0.11928 or 11.928%. Therefore, the NML is approx. +11.928% of Ideal. For Noise Margin High: (2.0921-2.5) / 2.5= -0.16316 or -16.316%. Therefore, the NMH is approx. -16.316% of Ideal.

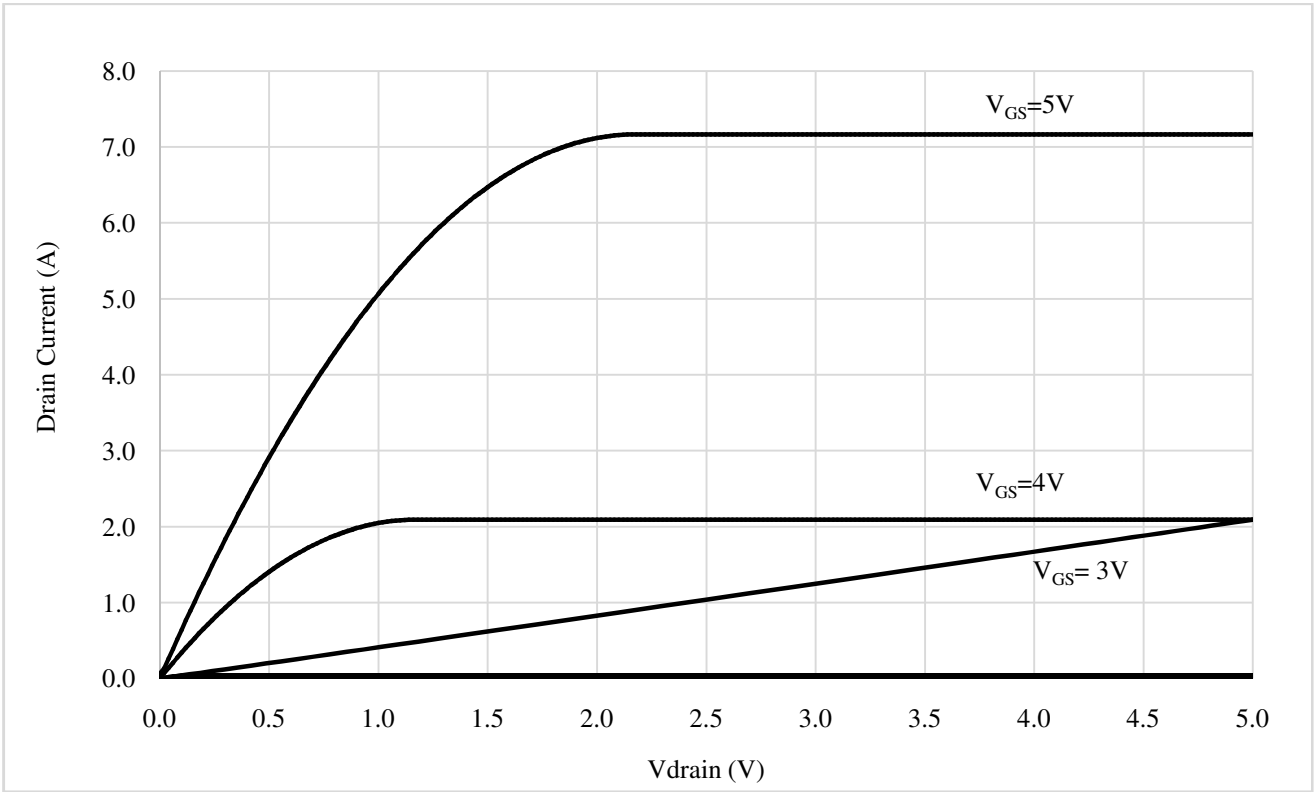

Figure-2: VI Characteristic.

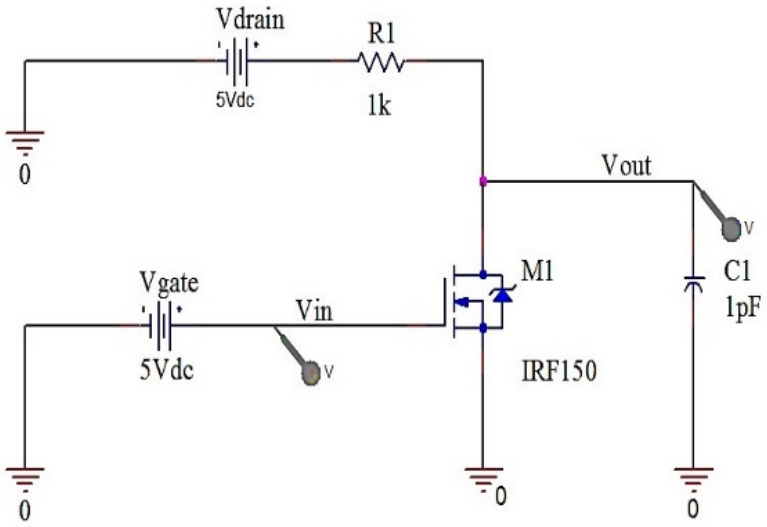

Figure-3: Circuit for VTF.

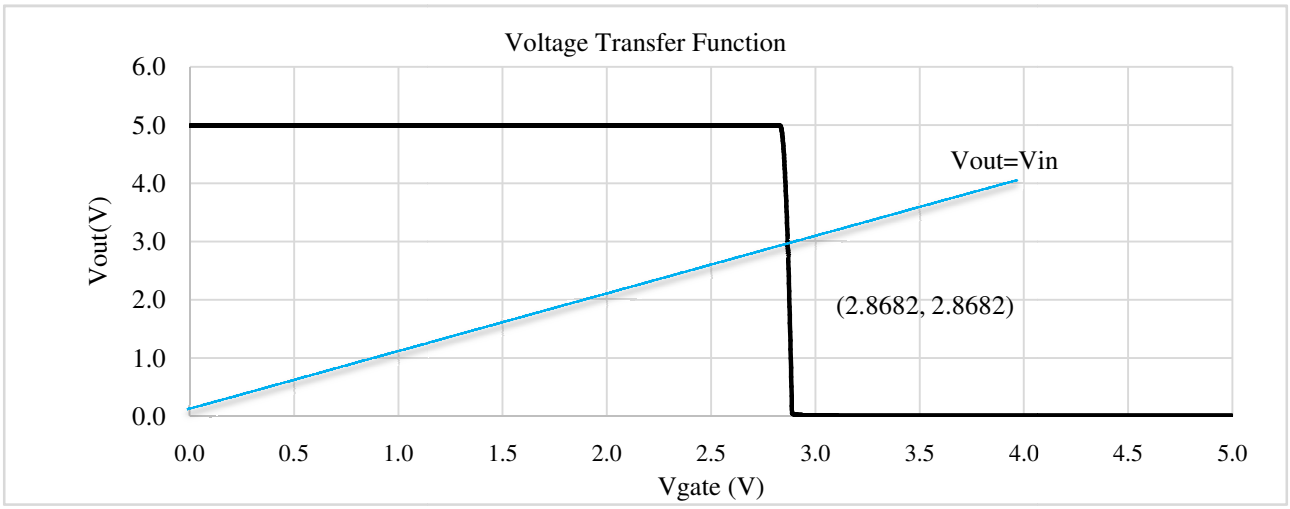

Figure-4: Simulation of voltage transfer function.

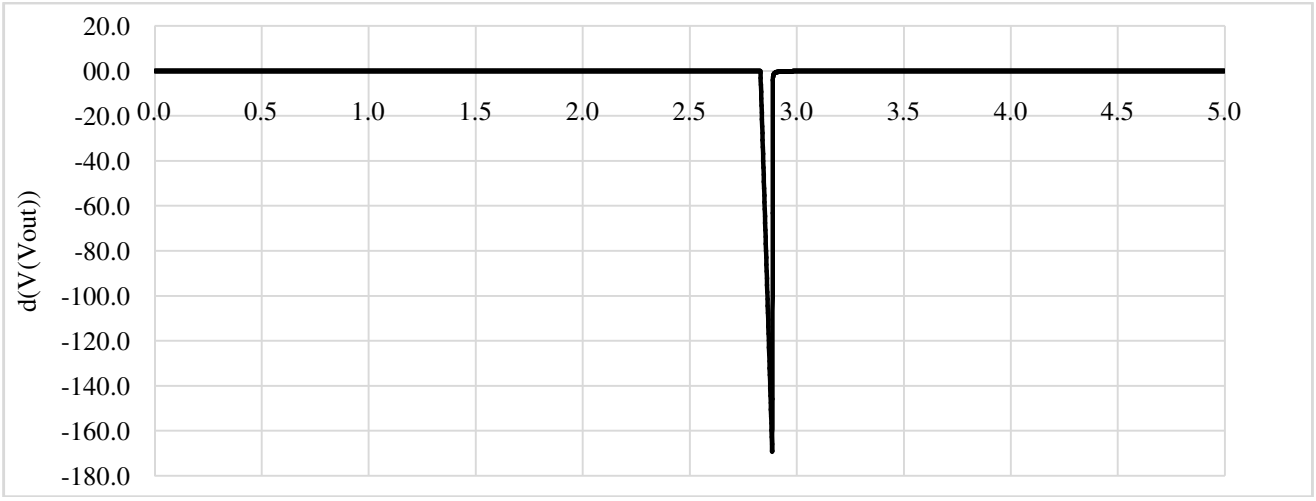

Figure-5: Simulation of derivative of Vout with slope = -1.

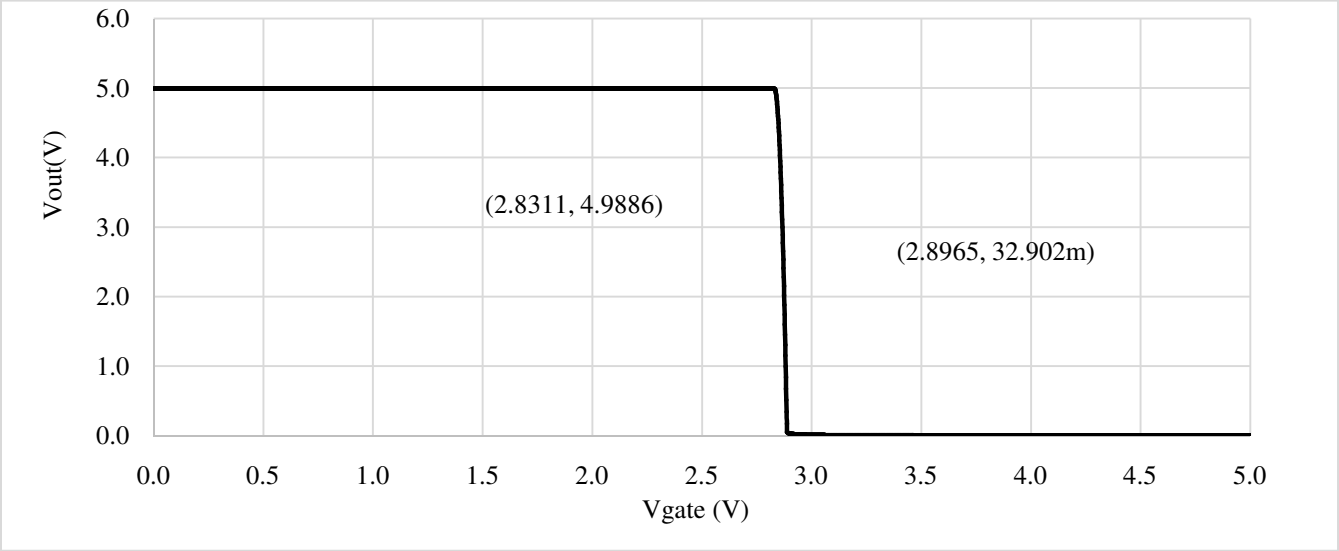

Figure-6: VTF with corresponding point from slope= -1.

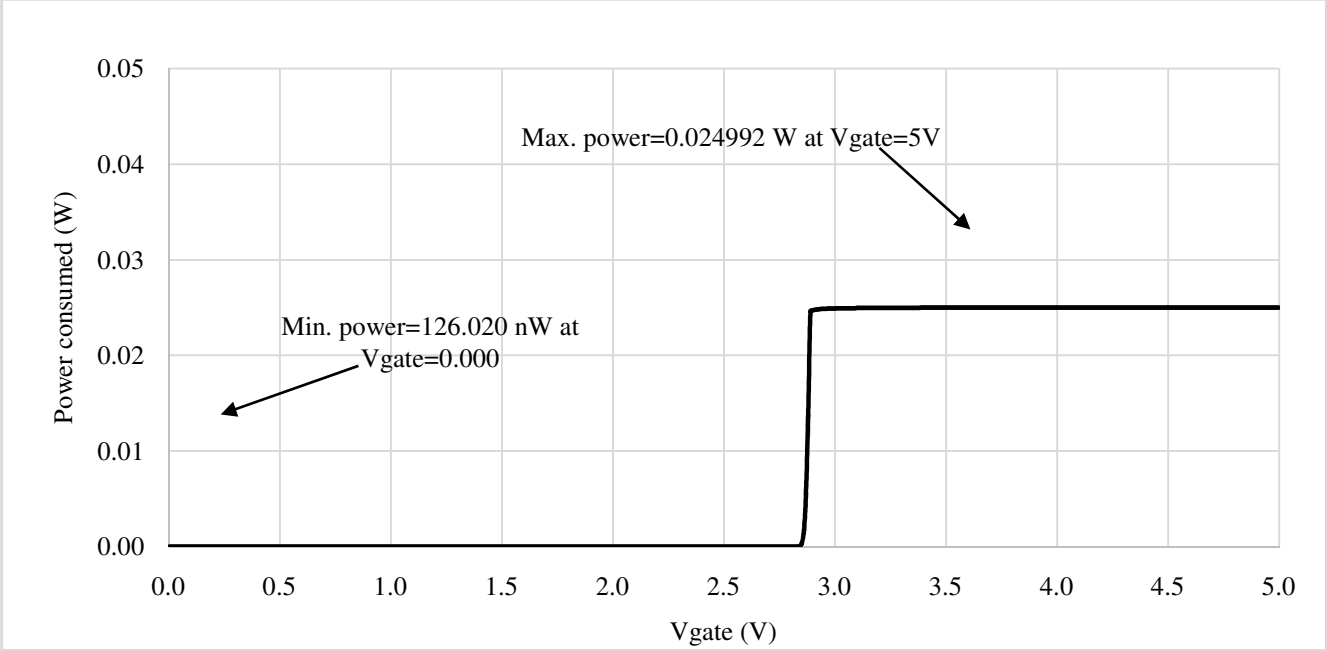

Figure-7: IRF150 Power consumption.

Using the same circuit diagram, the power consumed[11] by IRF150 is evaluated. The voltage probe at "Vout" is replaced bya power probe at Resistor, "R1" in above circuit connection and its corresponding simulation result is shown in Figure-7. From the figure,the maximum power consumed is 24.992mW and the minimum power consumed is 126.020nW. As observed, the minimum power (126.020 nW) is consumed when the MOSFET is inverting Low Input Logic (0) to High Output Logic (1). The maximum power (24.992mW) is consumed when the MOSFET is inverting aHigh Input Logic to Low output logic. The power 126.020 nW is consumed at zero input voltage (Vin=0), while24.992mW power is consumed at high input voltage (Vin = 5V).

Further changing the V_{DC} power source "Vgate" voltage to the threshold voltage determined in Figure-3, the small signal parameters of IRF150 was evaluated. Threshold voltage, V_{DC}= 2.8682V is used. Through the simulationthe gain is observed to be -1.143 with its input resistance of 1.0 Ohm and output resistance of 9.978 Ohm.

Analog and Digital Frequency Response of IRF150: To find the analog frequency response the bode plot of the circuit, an ac source V_{AC} with 1 V_{AC} was added. Maintaining the same threshold voltage of 2.8682V at Vgate of the MOSFET, the simulation was carried out.The circuit diagram is shown in

figure 8 and its corresponding simulation output is shown in Figure-10.

From the response the IRF150 behaves like a low pass filter with f*3 dB frequency of 55.857KHz.f*3 dB is the corner frequency in which the maximum voltage gain is reduced by 3 dB. The response exhibited higher gain with better response at lower frequencies from the corner frequency whereas poor response was observed at higher frequencies from the corner frequency. The frequencies below 10 KHz received higher gain allowing MOSFET to switch faster like an ideal inverter. The slope of the graph is given by, Slope= Rise/Run. Therefore, the Slope is 18.981dB/decade. Further, the digital frequency response of IRF150 was evaluated. The circuit diagram and its corresponding simulated response is shown in Figure 9 and 11 respectively. For the digital input, Vpulse is used with PER is 17.857 microseconds and PW is 8.9285 microseconds. From the response the corner frequency is found to be 55.857KHz which is approx. 56 KHz with Time Period as, T = 17.857 microseconds.

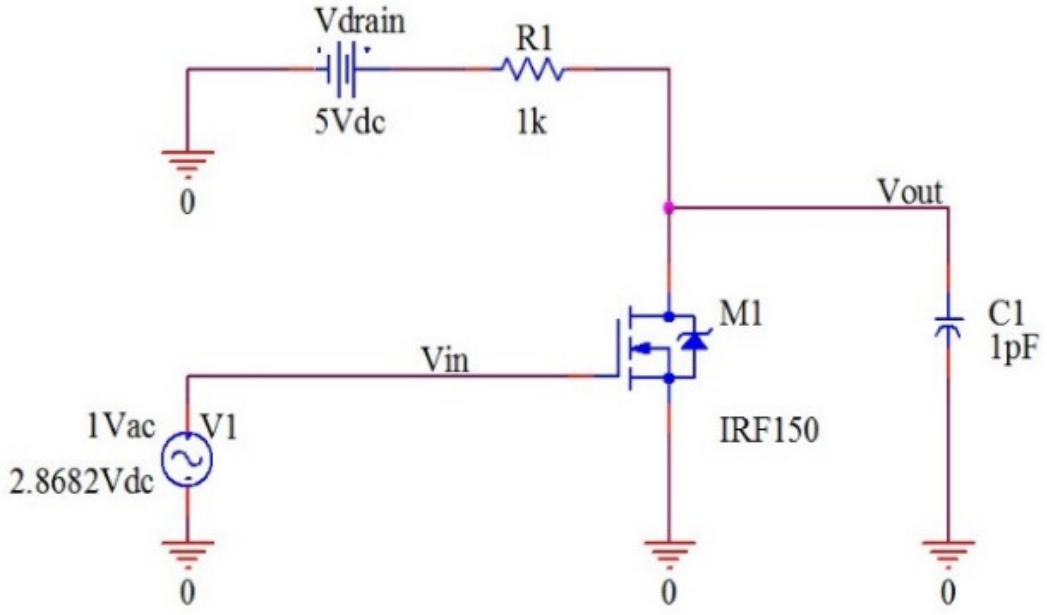

Figure-8: Analog response circuit diagram.

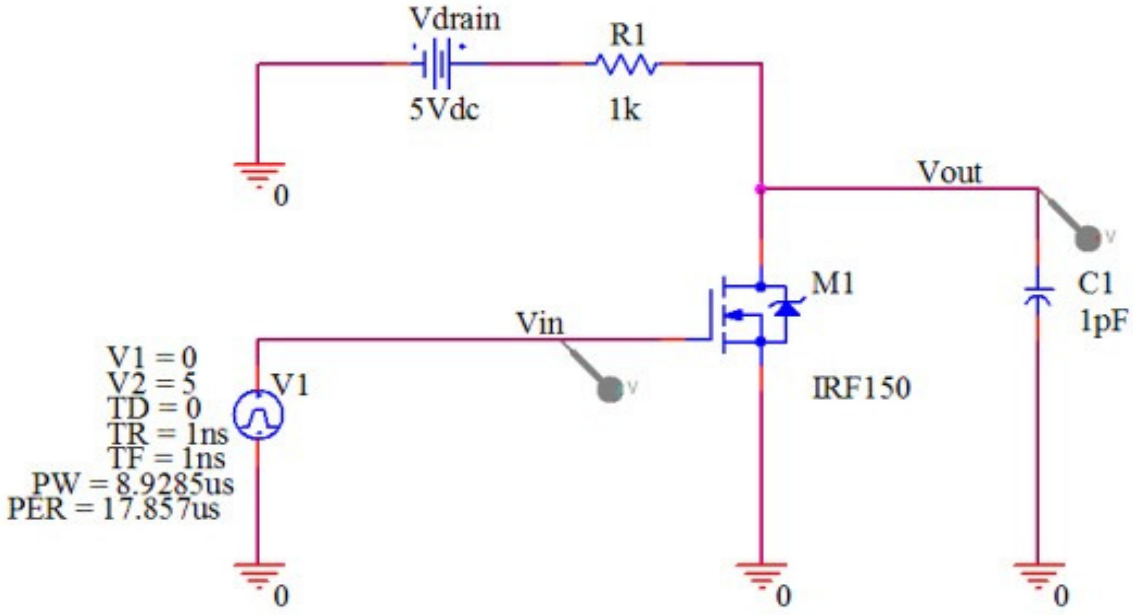

Figure-9: Circuit diagram for digital response.

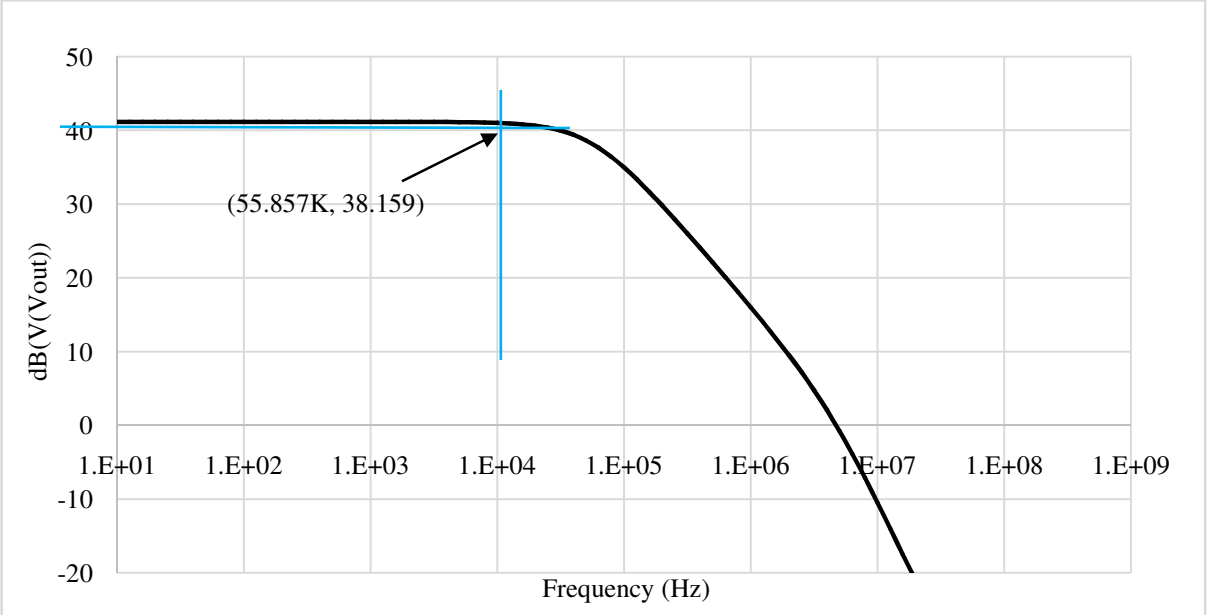

Figure-10: Analog frequency response of IRF150.

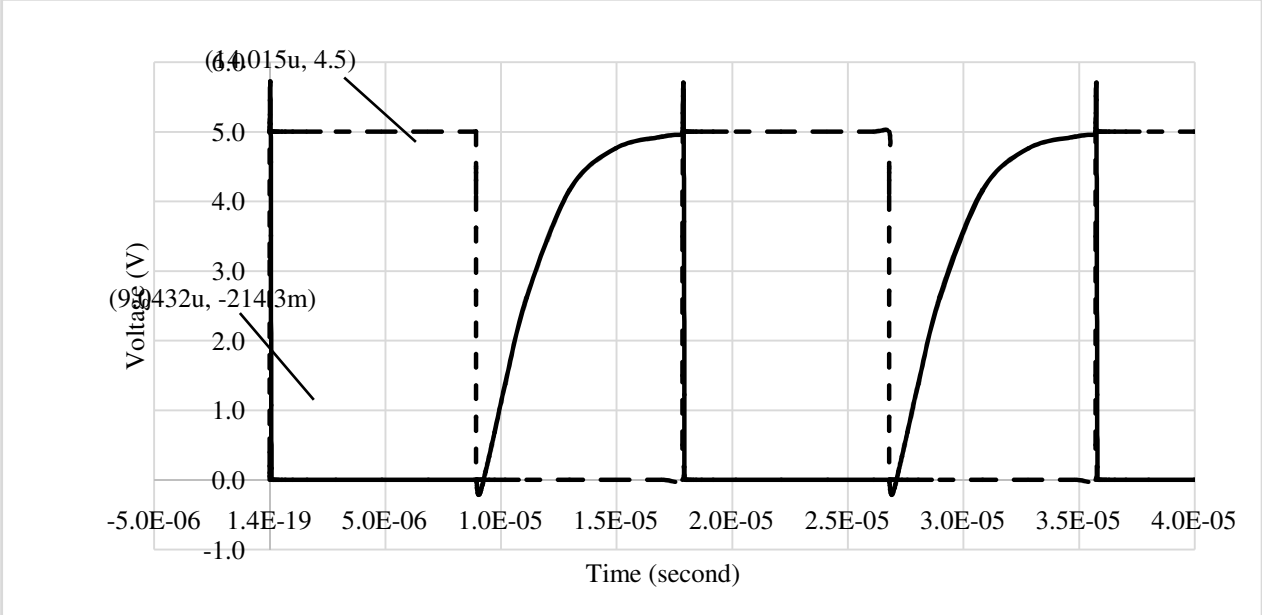

Figure-11: Result showing digital response.

From Figure-11, the dotted line represents the input voltage (V_{in}) and the dark straight line is the output inverted response (Vout). As observed, the IRF150 exhibits the property of an efficient inverter with output reaching over 90% of the operating range. However, this response can be improved with a lower input frequency. The rise time is (14.015-9.603) =4.412 us. The evaluated corner frequency is 55.857KHz which is approx. 56 KHz.

Further for better analysis the time period of Vpulse were varied extensively by decreasing its operating frequency to 5.6 KHz and increasing to 560 KHz. For 5.6 KHz, PW of 89.285 us is adapted with PER of 178.57us. The evaluated response is shown in Figure-12. From the figure, the response is much clearer and is comparable to an ideal inverter. The frequency (5.6 KHz), which is less than the corner frequency portrait better response with higher gain. For 560 KHz, PW of 0.89285us is adapted with PER of 1.7857us is adapted. At this high frequency which is greater than corner frequency has poor digital response as seen in Figure-13. Due to low gain at higher frequencies the IRF150 cannot switch fast enough to follow the input signal.

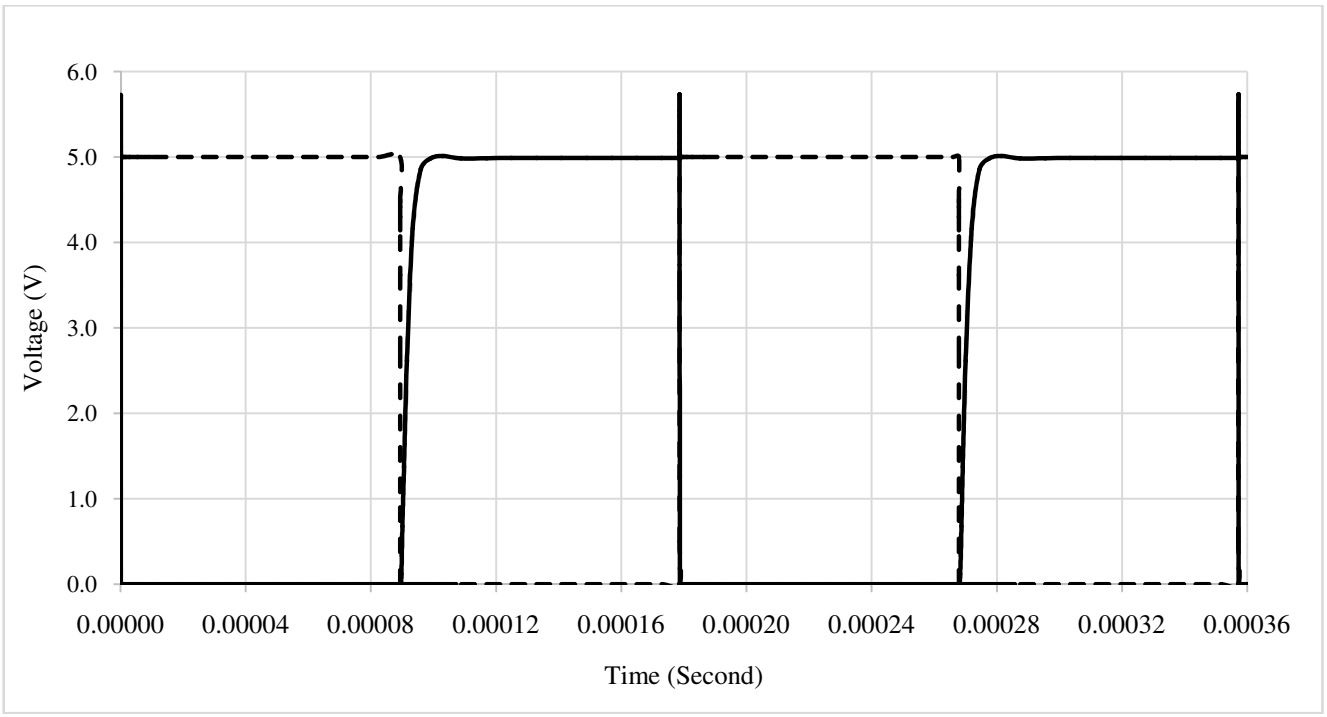

Figure-12: Response at 5.6kHz (.1 * corner).

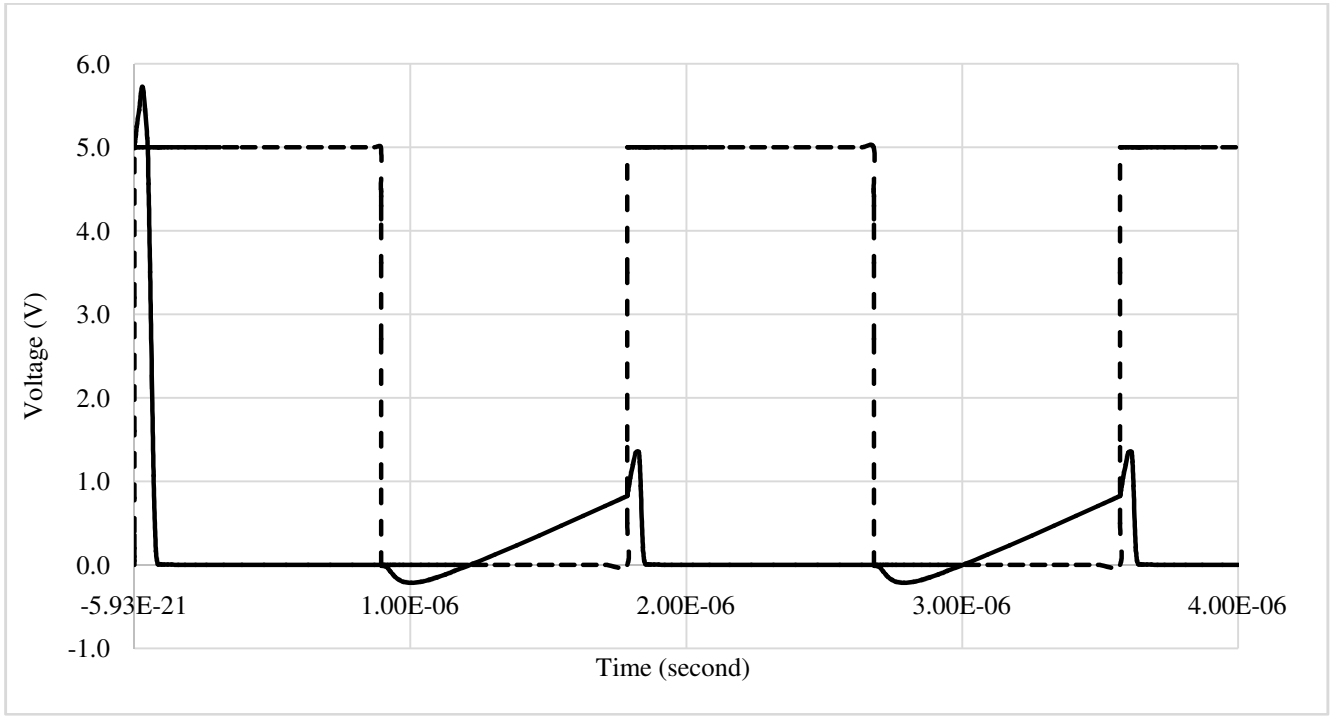

Figure-13: Response at 560kHz (10*corner).

Maximum Frequency of the MOSFET circuit: The maximum frequency is the frequency at which the output reaches to 90% of the operating range within the pulse width. Using corner frequency as the initial point the frequency was increased linearly until the output is 90% of V_{DD} (4.5V). When frequency, f is at 100 KHz the output Vout reaches to 4.5V. The graph in Figure-15 shows the maximum frequency of the MOSFET. When frequency, f= 100 KHz, the output Vout reached to 4.5 V which is a 90% of total V_{DD}= 5V. Thus, the frequency, f= 100KHz is a maximum frequency of MOSFET. The time taken by the MOSFET to rise from Vout Low Logic (0) to Vout High Logic (1) is 4.2905us.

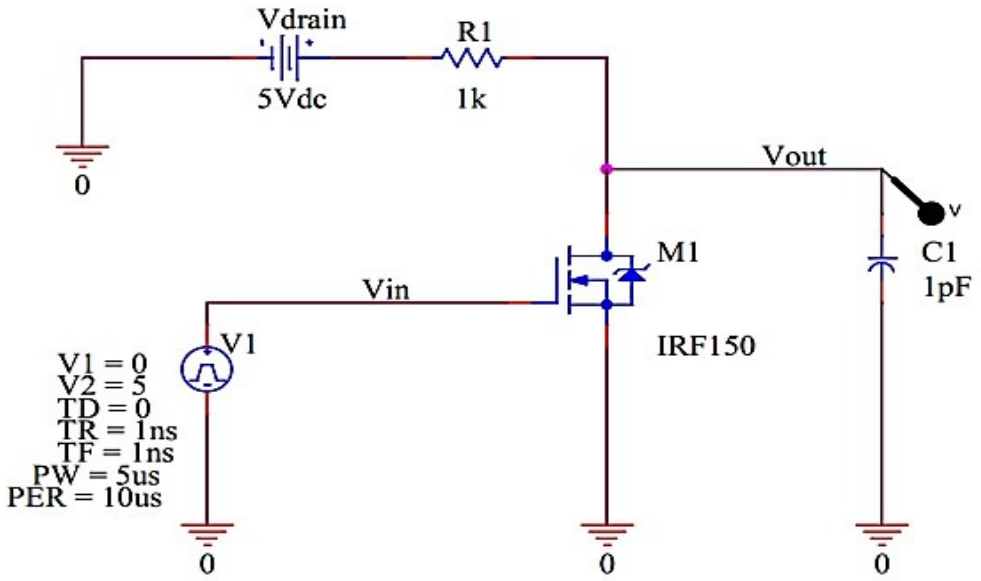

Figure-14: Circuit diagram for Maximum Frequency.

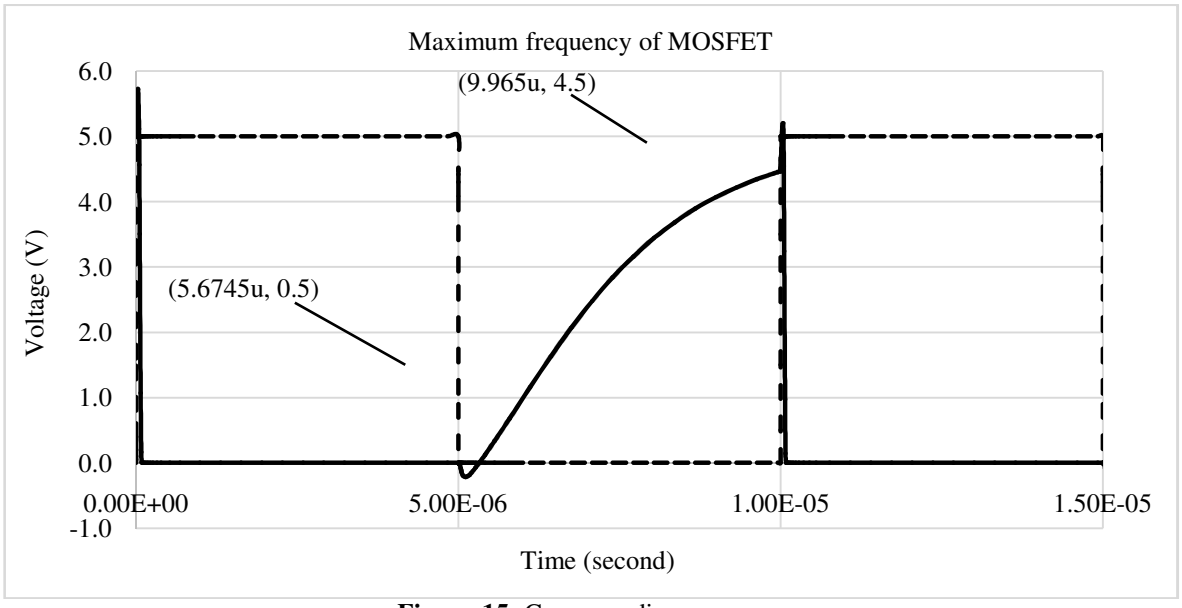

Figure-15: Corresponding response.

Conclusion

From the Characteristics Curve, the threshold voltage of P-spice MOSFET (IRF150) is 3 V. Logic threshold is the point where the input voltage (V_{in}) is equal to the output voltage (V_{out}). From the voltage transfer function, the switching point or logic threshold was found 2.8682V.The calculated the noise margin of IRF150 was evaluated to be Noise Margin Low of 2.797V and Noise Margin High of 2.0923V.The power consumed at V_{in} of 0V is observed to be 126.020 nW, while the power consumed at V_{in} of 5V is noted as 25mW.From the Frequency Response of the MOSFET, the circuit behaves like a low pass filter with f *3 dB of 55.857 KHz. The slope was found 18.975 dB/Decade. From the Digital Frequency Response of the MOSFET, it found that the frequency less than corner frequency gives the best digital response that is nearly to that of ideal inverter. Maximum frequency of the MOSFET is found to be 100KHz which gives about 90% of the total output.

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