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A Novel Approach to Design a Nano Metric Reversible Counter

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Abstract

Today's Technology that used to build computer circuits, because of the limit, unable to respond the human needs in the design of very fast and low-power computers. That's why scientists are looking for alternative technologies and one these technologies are reversible logic. The reversible gates and reversible logic are designed using reversible logic. The main advantage of reversible logic is obtaining is input vector from the output vector. In this paper the design of a Nano metric reversible counter has been studied. The circuit of reversible Counter is formed flip-flops and logic gates. In fact there are two schemes for reversible counters that use as a Nano metric reversible counter with Parallel Load capacity and concurrent clearance. In this paper, two approaches have been used to design a timer circuit and the proposed circuit characteristics were compared and the results are compared to each other.

Keywords: Reversible gates, reversible logic, Nano metric reversible counters.

Introduction

The Moore's Law is a part of the world of semiconductors, microelectronics circuits and the IT industry[1]. According to this low every 18 months the number of transistors used in microprocessors doubles. Half of gates of the transistors with a fixed silicon chip size could be the result of this legislation[2]. In fact this low represents an economic issue and impact on transistor performance too. This means that whatever the gate be smaller, transistors can switch faster and thus less energy would consumed.

Reversible logic and the gates that built with this logic is one of technologies that look pretty good to build future computers. Automated processing of information in any form is performed on digital and classical calculations. But there is less than a decade that a better and more powerful way for information processing is proposed, which is based on quantum mechanics[3,4]. This new method is associated with some features that make it very distinct from classical computing. These features include: superposition, interference, twisted and non-proliferation.

This paper examines the effects of these features. Structure of quantum computers becomes increasingly more technical and scientific and their developed design techniques such as modeling and combining it with DNA are applicable in quantum computing and also in other modern technology because of their reversible property[5,6]. Reversible logic plays an important role in the synthesis of quantum computing circuits[7]. Synthesis of reversible circuits using elementary quantum gates is different with the classic synthesis logic. The basic unit of quantum computing is a qubit which is superposition of zero states and one state.

A qubit is a unit of quantum information. Because the quantum gate unit is shown in matrix form, combinatorial algorithms for quantum circuits will always display in this form[8]. Variety of methods for combining reversible logic circuits is presented[9-11]. Quantum gates that are represented by a unit matrix have the potential to implement reversible logic circuits. Reversible logic circuits are separated by two features from other logical circuits: The number of output bits is equal to the number of input bits. For each pair of input expressions, the corresponding output is different.

Generally reversible circuits' characteristics are: Not losing information, the heat generated in the circuit, no wasted energy, equal number of inputs and outputs, zero power consumption and One-to-one correspondence between inputs and outputs of a circuit[12]. Due to many benefits of these circuits, since many designs for reversible logic circuits is presented.

In this paper we introduce two circuits of reversible nano metric counters and compare with similar counters circuits. Generally a register that through a series of preset states by applying the input pulse is called timer/counter.

In recent years, some research has been done on reversible logic counter with parallel load but in the nanometer counters with a synchronized cleaner parallel load has not been. Hoghparast[12] designed a 4-bit nanometer reversible counter with parallel load round with a minimum quantum cost and complexity. This design does not support simultaneous erasure. The circuit is presented in this article also has this capability. It will start with investigating of previous circuits and the components of the proposed counter's circuit, and then the two circuits are studied.

Basic concepts of reversible flip flaps

This section the components of a reversible circuit is investigated. Since the purpose of this paper is to design a reversible counter circuit only the principles of reversible JK and D flip flop is explored.

JK reversible flip-flop: Flip-flop is the main component of reversible circuits that many of these circuits can be designed using this. JK flip flop is used as the main part to store the bits of reversible data. Reversible JK flip-flop includes one Fredkin gate and one Feynman gate that used in the design of sequential circuits[12].

Characteristic equation of the JK flip-flop is designed using two Fredkin gates and one Feynman gate, Feynman gate is used to copy output bit. The JK flip-flop is shown in Figure 1. The designed circuit is highly optimized in terms of reversible gate count, constant inputs and unused outputs. CP input refers to the clock. It can be easily verified that the construction in accordance with the desired properties can be practical with the JK flip-flop positive edge excitation. Reflect of the feedback of connection from output to input is needed because the JK flip-flop has "no change" conditions. The JK flip-flop using reversible gates is shown in figure-2.

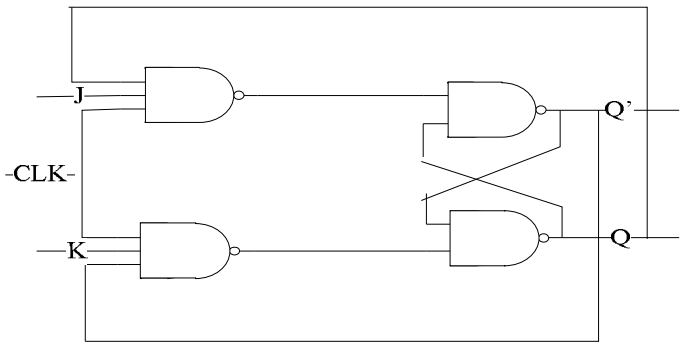

Figure-1
Designed JK latch with the conventional logic gates

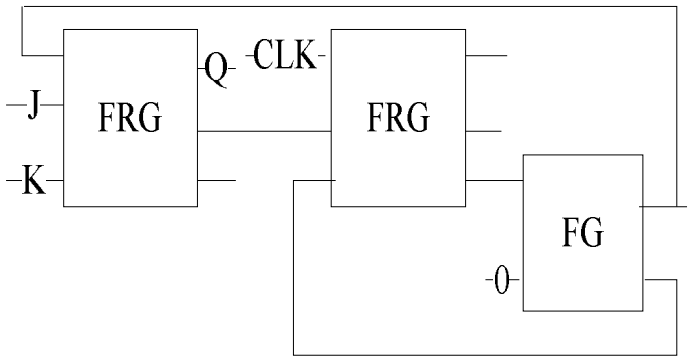

Figure-2
Implementation of JK latch using reversible gates

Reversible D flip-flop: D flip flop used as the main part to store data bits of reversible data. Reversible D flip-flop includes one Fredkin gate and one Feynman gate that used in the design of sequential circuits. Reversible D flip-flop is Master and Slave. Figure-3 shows the internal structure of the D flip-flop show in typical performance. The designed circuit is highly optimized in terms of reversible gate count, constant inputs and unused outputs. CP input refers to the clock. It can be easily verified that the construction in accordance with the desired properties can be practical with the D flip-flop positive edge excitation. Reflect of the feedback of connection from output to input is needed because the JK flip-flop has "no change" conditions. Figure 4 shows the implementation of D latch using reversible gates.

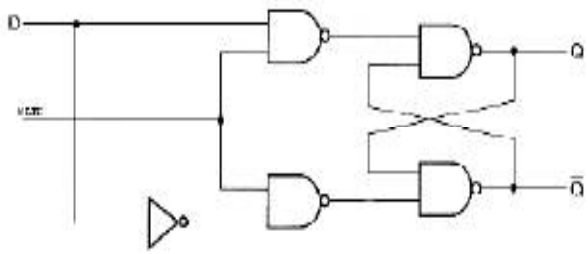

Figure-3
Design of D latch using common gate logic

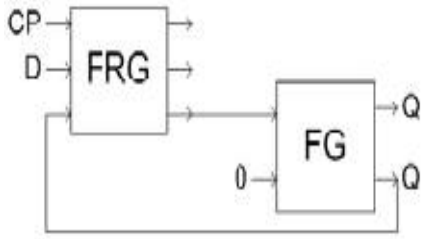

Figure-4
Implementing of D latch using reversible gates

Quantum cost for the two circuits in figure-4 and figure-2 is as follows:

$$QC_{(D-FF)} = 2QC_{(FRG)} + QC_{(FG)} = (2 * 5) + 1 = 11 \quad (1)$$

$$QC_{(D-FF)} = QC_{(FRG)} + QC_{(FG)} = 5 + 1 = 6 \quad (2)$$

Related Works

To date, only one study has been done on reversible counters. In Haghparast [12] design a reversible 4-bit nanometer binary counter with parallel load is designed with minimum complexity and quantum cost. The proposed circuit is the first design for a 4-bit binary counter with parallel load. This counter, receive 4-bit input data and offering this data to the next level using D flip-flop. The main reversible gates used to design the circuit are FG, FRG and PG gates. The designed circuit using these optimum gates and minimum unused inputs and outputs is reversible. The logic circuit of a 4-bit binary counter with parallel load is shown in figure-5 and the designed circuit of a 4-bit binary counter with parallel load is shown in figure-6. The table function of figure 5 is shown in table-1.

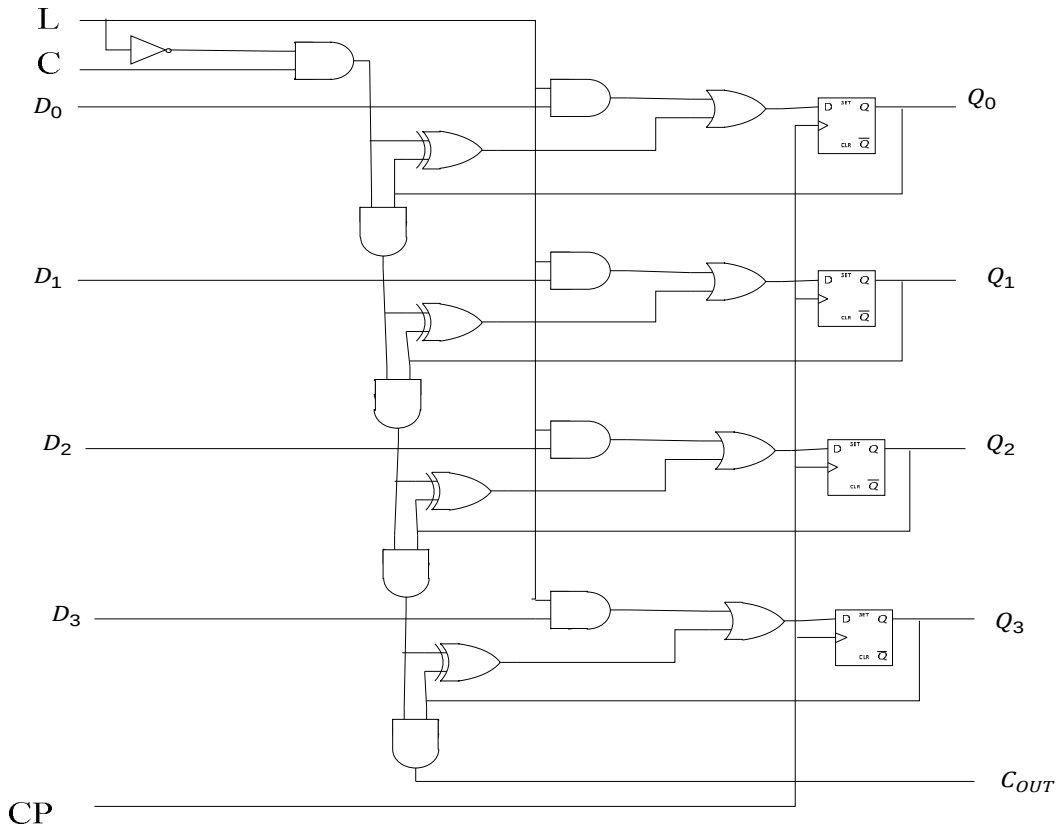

Figure-5
4-bit binary counter with parallel load

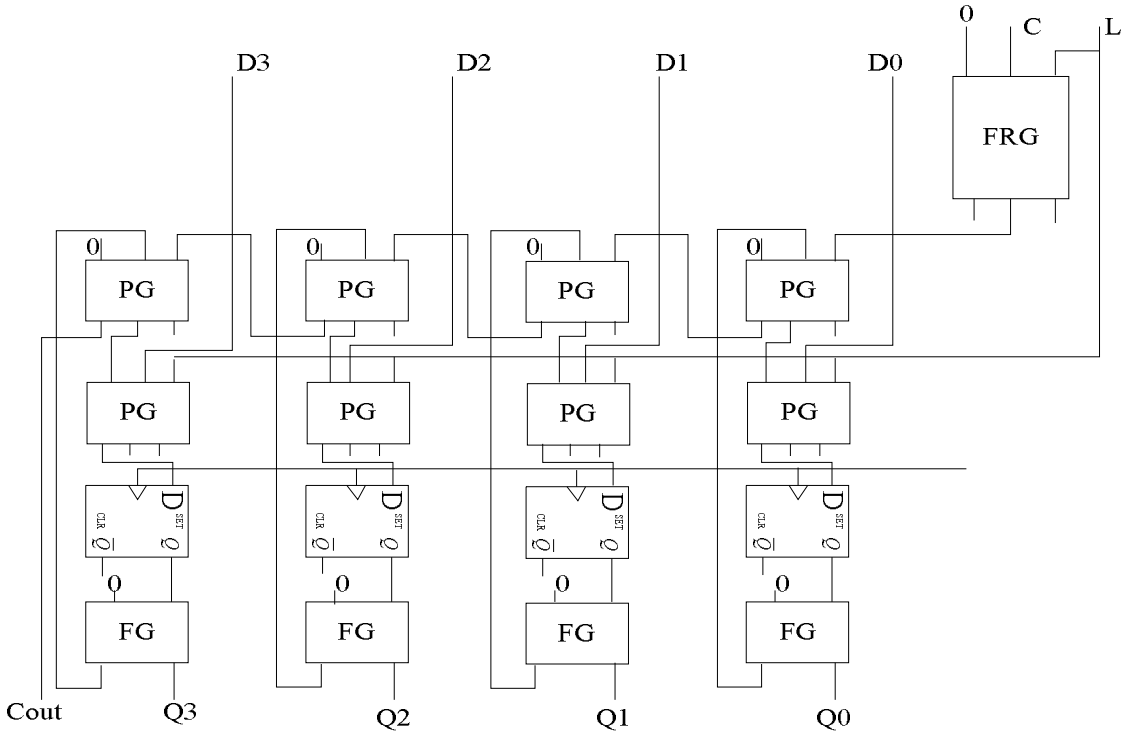

Figure-6
Reversible 4-bit counter binary with parallel load

Table-1
Table function of figure-5

Clock	Clear	Load	Operation
↑	0	0	No change
↑	0	1	Increment
↑	1	0	Load input

Proposed design

The circuit can be designed to modify to be more convenient than previous designs in terms of quantum cost, number of used gates and the number of unused output. Two circuits are presented in this paper, which has significant advantages over circuit of the earlier part and two different approaches have been defined.

First approach of design the circuit of reversible 4-bit binary counter with parallel load and concurrent clearance: The circuits of counter can be implemented by reversible logic circuits[14,15]. Counter with parallel load can be preset value. Load signal indicating that data will be transmitted to the counter and clear signal reset the counter to zero. The branching output signal can be used for higher level. The proposed 4-bit counters can be used in design of any n-bit counters, $2 \leq n \leq 16$. Logic circuit of counter with parallel load and concurrent clearance is shown in figure-8.

Even if the pulses are applied to the C input, it would be no change in output if all clear, load and increment inputs be 0. If the clear and load inputs are kept in 0, the increase input controls the functionality and outputs to transition to the next binary number per clock. When the input load is 1 if the clear input is Inactive but increment input is 0 or 1, the input data will load in Flip-Flops. Applying clear input the register will be 0 regardless of the of load and increment inputs.

Summary of counter with parallel load and concurrent clearance: Inputs are transformed into outputs if Clock and Load are activated. The flip-flop outputs are zero if Clear and Clock are activated. Output increases by one unit if the INC and Clock are activated. All flip-flops are one if Preset is enabled (zero).All flip-flops are zero if Clear is enabled (one). Preset and Clear do not required Clock. If the Load and Clock are disabled, even if a different number given to the inputs, the output does not change because Load the disabled. If there is not a Clock Pulse, there are no outputs regardless of the inputs. Regardless of the Clock Pulse, the final output is activated if Preset is enabled just for a moment. Regardless of the Clock Pulse, the final output is zero if Clear is activated just for a moment. Carry Out is activated when the output is reached F. After this time, the branching output is activated for a moment and then again it is zero.

Table-2
Results of Figure 7

Number of gates	Unused output	Quantum Cost	Fixed input	Total of rational calculation
15	9	40	7	$5 \times \delta + 11 \times \beta + 27 \times \alpha$

Second approach of design the circuit of reversible 4-bit binary counter with parallel load and concurrent clearance: In the second approach, the count will not change but the shape of the circuit change a little in order to improve implementation cost[16,17]. In this circuit, instead of using Clear input initially applied to the K input of JK flip-flop, it is connected to the Clr input of JK flip-flop. In which case Clear input is zero, flip flop is disabled and output will be zero. Figure 8 shows second approach of the circuit of reversible 4-bit binary counter with parallel load and concurrent clearance. Table 3 represents the result and calculations of designed circuit with second approach.

Table-3
The results of figure-8

Number of gates	Unused output	Quantum Cost	Fixed input	Total of rational calculation
11	7	31	5	$5 \times \delta + 10 \times \beta + 21 \times \alpha$

Continue to explain the comparison between the features of designed circuits using these two approaches and the circuit presented in 2011 which mentioned as earlier design in this paper. In this section, five properties are examined: The number of gate, unused output, quantum cost, fixed input and total of logic calculations. These are important features in assessing the properties of reversible circuits which have determined in mentioned two approaches and previous plan and are given in table-4.

Table-4
Comparison of 5 features between two approaches ofcounters circuit design and previous design

Circuit title	Number of gates	Unused output	Quantum Cost	Fixed input	Total of rational calculation
Previous plan	17	18	41	9	
First approach	15	9	40	7	
Second approach	11	7	31	5	

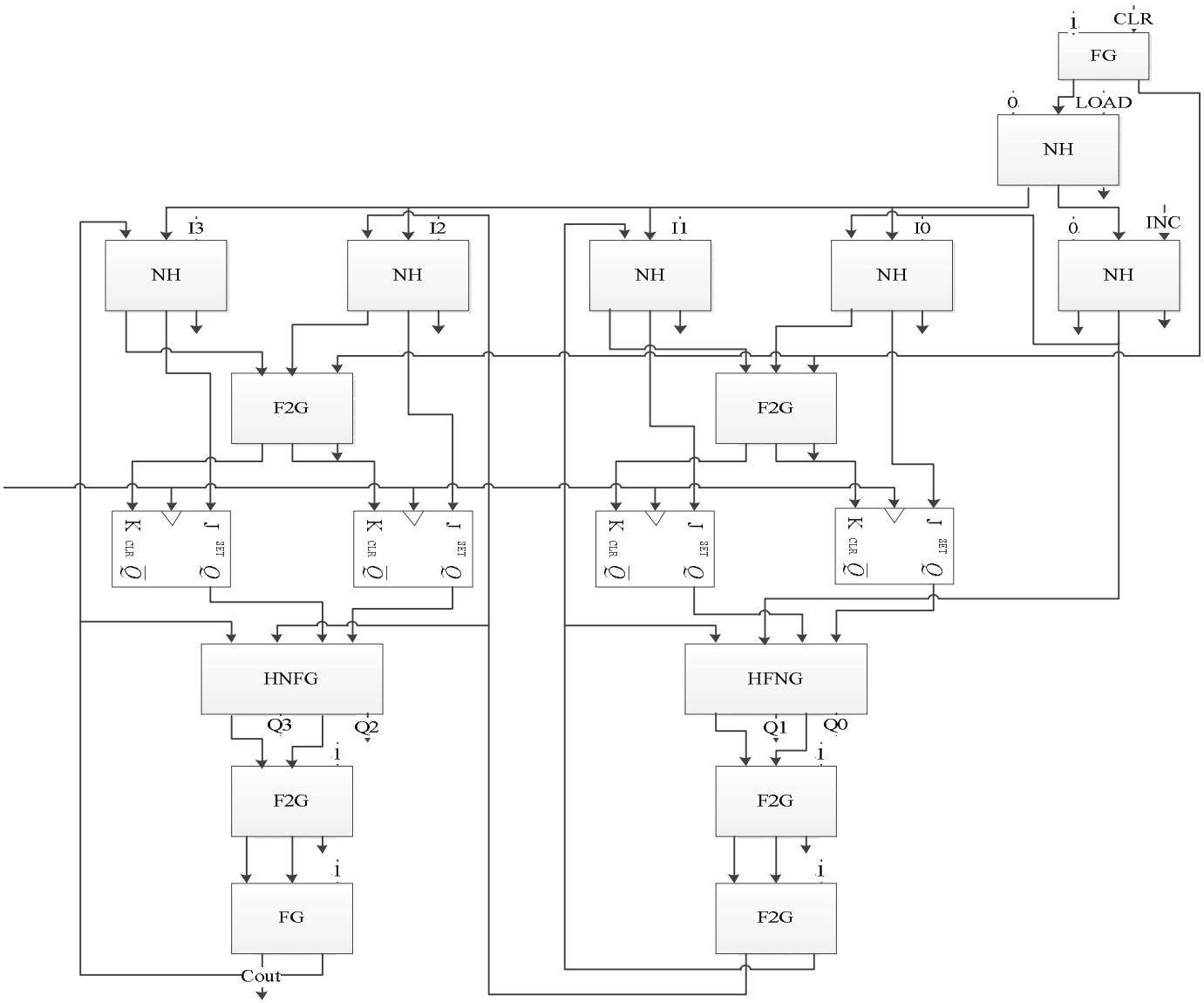

Figure-7
First approach of reversible 4-bit binary counter with parallel load and concurrent clearance

Human need for computer increased day to day and this manmade has found important and sensitive position in lives[18]. Using computers in different fields of life, it became clear that people need more quickly computers than previous ones and computer designers have tried to increase the speed of computers as possible[19]. In the design and construction process of a computer, addition to intelligence and creativity in design, the technology that used for implementation is also very important.

It is shown from different perspectives to build and deploy super-fast computers, today's technology that used in the manufacture of computers is not applicable and modern technologies are needed. Reversible logic due to the properties mentioned in this paper, such as not wasting energy can be the best alternative for today's technologies. With that said, activity in the field of modern computer design using a reversible logic is necessary than ever. Counter circuit is relatively one of complex circuitry inside the processor, which the optimum design can have a significant role in computer performance. In this paper we have used every endeavor to design a reversible counter circuit. According to our information this circuit is the second circuit for reversible counter with parallel load, except this is capable of concurrent clearance. Due to the great importance of circuits of arithmetic operations in the computers' processor the investigation on the design of mathematical circuit with reversible logic will continue in order to possible the optimized circuits for practical implementation in the near future.

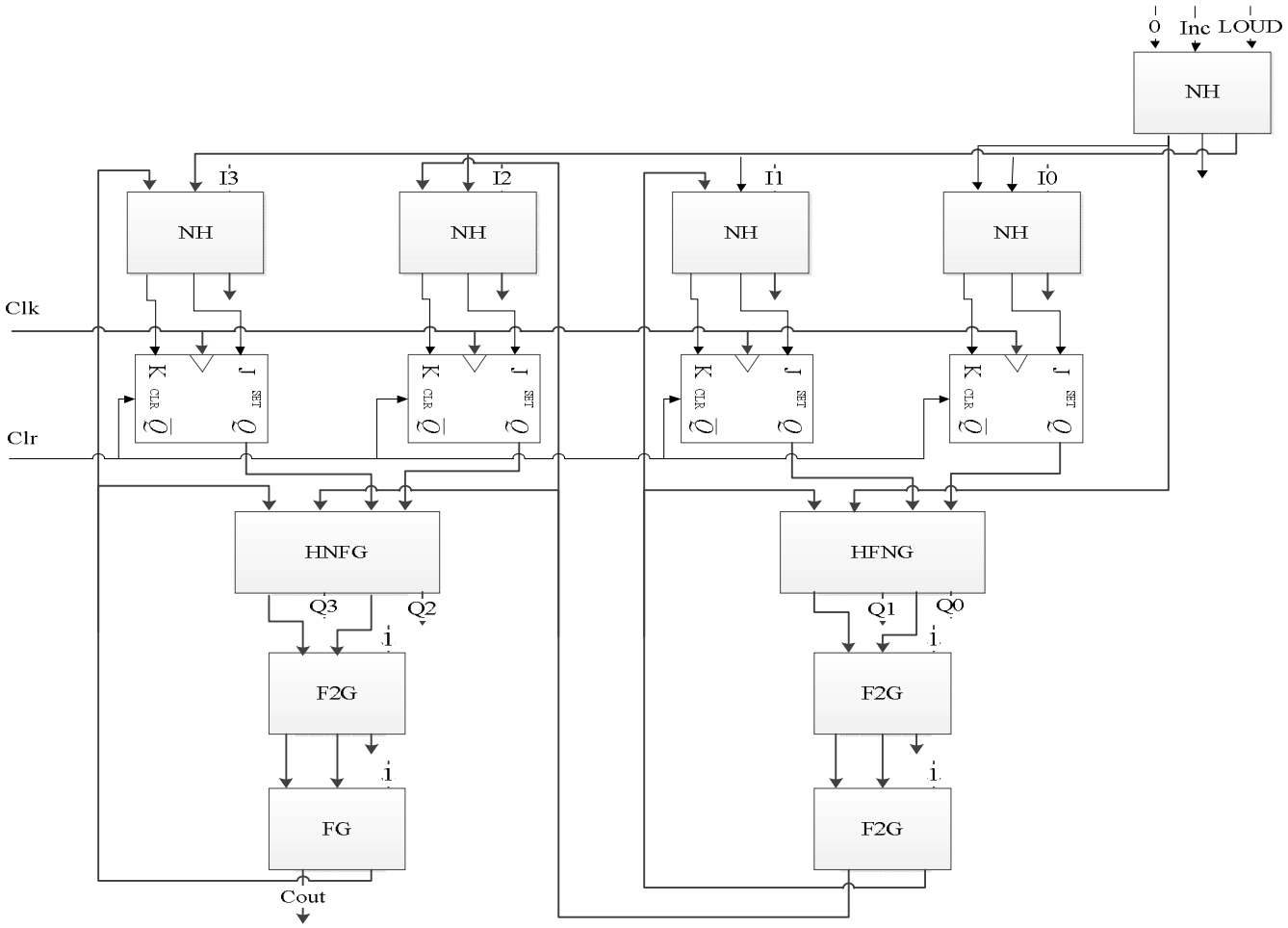

Figure-8
Second approach of reversible 4-bit binary counter with parallel load and concurrent clearance

Conclusion

This paper presents to investigate on reversible logic gates and reversible circuits. There are many advantages which cause to put the reverse logic gate into action[20]. The most important advantages of reversible logic can be not vesting energy bans able to recognize inputs produced from out puts. The design of Nano-meters reversible counters is categorized in two different types. This circuit is composed of flip-flops and logic gates. Counter with parallel load can be preset value. Load signal indicating that data will be transmitted to the counter and clear signal reset the counter to zero. The branching output signal can be used for higher level. In another view of this design, instead of using Clear input initially applied to the K input of JK flip-flop, it is connected to the Clr input of JK flip-flop. In which case Clear input is zero, flip flop is disabled and output will be zero. Figure 8 shows second approach of the circuit of reversible 4-bit binary counter with parallel load and concurrent clearance. Table 3 represents the result and calculations of designed circuit with second approach.

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