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Low-resolution Image Processing based on FPGA

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Abstract

Today, development of different methods such as scanners and digital cameras for receiving discrete data has led to high application of image processing. Images resulted from the discrete data have some noise and the distance among samples within the image might seem blur and it decreases the resolution of image. Image processing refers to a set of operations and methods used to decrease disadvantages and increase visual quality of the image. The issue of evaluating quality of images is one of the most common issues related to image processing algorithms. Resolution recognition is a criterion for the image acceptability; it also declares efficiency and acceptability of many of the algorithms associated with the image. The present paper intends to study low- resolution image processing based on FPGA.

Keywords: FPGA, low-resolution image, image processing.

Introduction

Image processing refers to a set of operations and processes which are done in different fields related to visual analysis. Image processing might increase or decrease image resolution. The specific meaning of image processing refers to any kind of signal processing whose input is an image such as a photograph or a frame of a video. The output of the image processing could be an image, a set of specific signs, or variables related to the image. Usually, image processing techniques treat the image as s two-dimensional signal and apply standard techniques of signal processing to them. Image processing usually refers to digital processing of the image, digital processing is one of the branches of computer knowledge and it deals with digital signal processing representing pictures taken by a digital camera or scanned by a scanner. Image processing has two main branches: image improvement, and vision of the device. Image improving consists of methods such as applying the blurring filters and increasing contrast for improving visual quality of images and getting ensured of their true demonstration within the target space (such as the printer or computer screen)[1].

The technology of multi-programmable switch array has made a new revolution in the digital design field. The concept of digital design has confronted a great evolution in the fields of architecture, design volume, speed, and type of attitude toward digital design. Today, FPGAs (field programmable gate array) provide an opportunity for designers to fulfill their digital design based on the required volume and complexity. In fact, FPGAs are the new generation of programmable digital integrated circuits. Speed of implementation of logic functions in FPGAs is very high and in the nano-second range. FPGAs refer to a chip made of a high number of logic blocks, communication lines, and input/output bases settled beside each other in an array-form. Lines of communication that make a relation among logic blocks are made from programmable switches. Depending on their type, some of the switches are programmable only once and some others are programmable for several times. As it was mentioned, FPGAs are applied for implementing fairly complicated and digital functions that need high processing speed. The processing speed of FPGAs is considerable higher than that of the other systems. FPGAs include separate hardware whose task is to process data. Moreover, decreasing the required hardware and also simple-standard programming are the advantages of FPGAs. Specialized capabilities of this software have increased FPGA capabilities, and most of the time, it is the processor is used in processing circuits. Also, it has many other amazing capabilities that provide the opportunity for doing an integrated, low-volume, optimized, and quick design. High-speed of FPGAs makes them appropriate for doing heavy processing activities such as sound and image processing[2].

The present paper with the purpose of low- resolution image processing aims to study low- resolution face recognition in the image processing based on FPGA. Face recognition is a successful application of image analysis. Low resolution of the image is a vital issue considered by researchers. Improving the image is an inevitable stage for improving visual features of images with low contrast. The resolution of some medical and aerial images is so low that necessary details are not reflected in them. Therefore, the resolution needs to be improved. The purpose of improving image is to reveal necessary features of the image; these features are unclear in the main image. In fact, low- resolution images problem is common in various processing devices and the performance of existing algorithms have not been successful for solving this problem. In order to address this problem, a strategy has been presented for getting aware of the relation between the image and low/high resolution. Based on the codes created in VERILOG via the modeling, FPGA is used to process images. Quick and correct processing of visual data is provided in this system. Laboratorial

test results indicate that in this research, FPGA is the best method for processing the image. It highly improves quality and clarity of blurred images and photos which have been taken with a tremor. There are different parameters related to designing image processing systems that influence the best choice of the applied hardware. Sampling speed, data transmission rate, processing computation speed, easy of designing, and low cost of the hardware are some of these parameters. According to the explanations, it could be mentioned that FPGA is a better choice for implementing image processing applications. This is an automatic method for optimizing, editing, and adjusting color of photos. It provides tools for improving quality and color, as well as editing photos[3]. It automatically solves problems related to contrast and whiteness of photos. It also is able to remove the noise of photos and redness of eyes in face photos. This software saves the performed adjustments and processes, and then it applies them as profiles to the next photos one would aim to edit. Also, the processes could be applied to several photos simultaneously. Face recognition system is applied in order to recognize an individual through a digital photo or a video frame. A solution suggested for this issue is to compare face features with the whole of the face. Visual data could be used for operation implementation in this field. To do so, the camera is installed in a fixed place and the place of the image will be enlarged, while the face which is getting edited stays at the same size. In order to recognize face from the camera, it is possible to solve the problem of low resolution of the face by making changes such as enlightening the face. Speed increasing in processing two dimensional and three dimensional images is possible via FPGA method. The application of this method is obvious in two-dimensional and three- dimensional low resolution images recovery, images dividing, recovering the primary image, and matching the primary image with image background and simulating the image. Implementing FPGA method has many advantages including accordance of this method with algorithms and enough accuracy for protecting effects of the mathematical model. Different variables could be used along with a similar hardware via uploading a new programming in FPGA. Through this method, image processing in applications that pay attention to the "real time" has been demonstrated[4].

Moreover, face recognition through image is possible in spite of different states such as rotation or occlusion in low-resolution images. Recognizing the visual quality and determining decrease of visual quality are key points considered in evaluating methods of image processing such as compressing, noise removing, and water marking. Traditional methods such as mean of squares do not highly consider objects structure in PSNR and/or MSE of image error and role of pixel location in the image and different impacts of pixels with regard to their location on the human' eye. In this research, a high-resolution image processing algorithm has been presented. It takes advantage of this algorithm to turn the low- resolution facial image into a high- resolution facial image. If the image has a proper illumination, the algorithm will be useful.

Figure-1
Blur images

In fact, problems such as images being faded and blur are related to the low- resolution problem. To solve this problem related to low- resolution of the image, super- resolution algorithms have been presented, however, the quality of these algorithms might not be satisfactory, and in the image resolution is considerably low. In order to solve the problem of low-resolution images, the lost visual data of the image should be recovered. Therefore, the available algorithms are categorized based on two strategies including posteriori approach and example- based approach. These strategies evaluate error in order to retrieve the low- resolution image and gain a high-resolution image. Through image retrieval, low- resolution image is required as a result of lack of visual data. Data limitations are used to compare images via calculating distances in the space of low- resolution image for processing image high-quality and clarity. Face recognition system consists of three main stages for image processing. Face recognition consists of recognition and separation of a region of the face from the whole image of the face. Features related to an area of the face separated from the image indicate features of the whole face image. The features include normal features such as fixed lines or other facial features related to mouth, nose, and eyes. Face recognition is possible via matching the input image with images of different faces available in the databases[5].

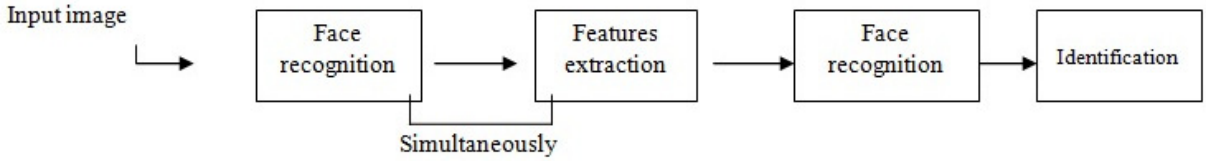

Figure-2
Face recognition system

Face recognition system is divided into two categories: Total methods that include a range of image features. Processing some of the image features is possible via this method. Moreover, statistical characteristics of face are analyzed based on a set of images. Features based on face recognition are extracted via method of fixed points available on face. Then, features are used for categorization.

Methodology

MATLAB software is used to process images. It has a high efficiency in image processing. MATLAB has the ability to process two images taken from the database. In fact, comparing images is a strategy for image processing. The two images analyzed by MATLAB software consist of an image with high-resolution and clarity and an image with low- resolution. These two images could provide a test input so that one could use it as the input in the verilog model.

RLSR algorithm is effective for applying the available information in the training stage. Moreover, SR approach has been presented based on this algorithm in order to recognize face. Mostly, methods presented via this algorithm are useful for retrieving low-resolution images. According to this algorithm, first, the image spaces with high and low resolutions are determined, and then this relation helps retrieving low-resolution images and gaining high- resolution images. Applying this method has many advantages. SR algorithm is effective for retrieving low- resolution images and solving problems related to low-resolution images. Linear clustering method confirms linear relation of data in each cluster. The method of learning the relation based on linear clustering could control complicated nonlinear cases. In this relation, R is normal for all face images with low resolution.

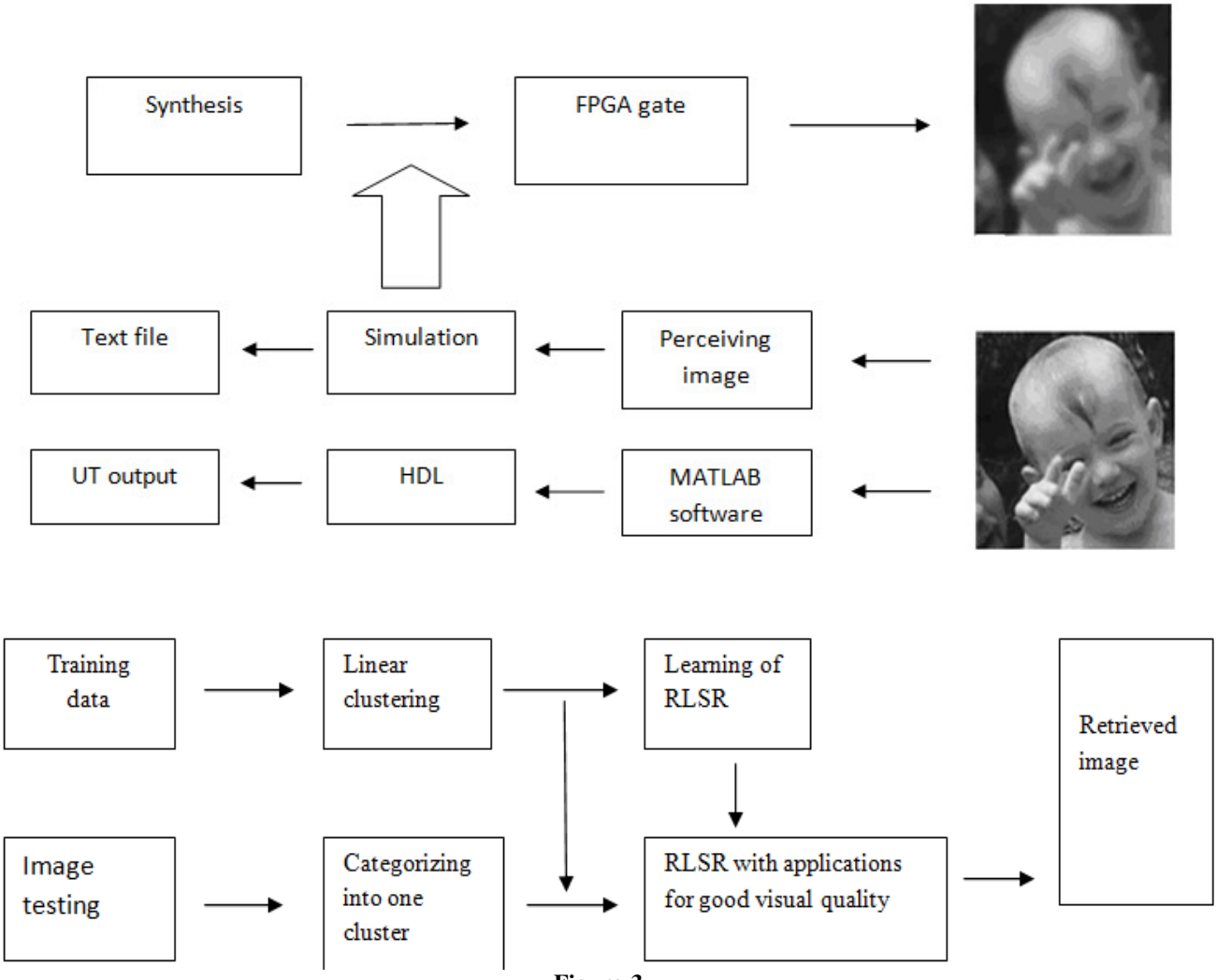

Figure-3
Block diagram of RLSR

Training phase: In figure-3, training phase consists of two stages called linear clustering and relation learning. In the first stage, a clustering algorithm has been presented as the pre-processing stage. After linear clustering, high and low resolution images are linearly settled in a cluster in pairs. It means that a high-resolution image and a low- resolution image are linearly settled in a cluster in pairs. Finally this relation could be demonstrated by a matrix. In the second stage, the relation is demonstrated by achieving a high-resolution image through a low- resolution image. In this field, a standard database is used for high- resolution image. All the images are considered based on a light homogeneous background with the other objects in the opposite direction. Files format is JPEG. In this database, images related to the children are located. In order to make images with very-low resolution, high- resolution images should be considered and size of high-resolution images should change[6].

The overall structure of FPGA: FPGA consists of a series of logic elements which are not limited for a specific activity as well as programmable connections. Therefore, both logic blocks and connections among them are programmable.

Logic blocks, resources integration for creating connections, and input/ output blocks are the three main components of FPGA structure. The structure and content of logic blocks could be very simple (such as NAND gates) or very complicated (such as MUX or Table Look-Up with a flip flop). First, the circuit which should be located on the FPGA needs to be divided into equal components or logic blocks content. Second, the base clocks are connected to each other in order to achieve the real circuits. The elements used for connections are usually located among logic blocks and are made up of metal pieces connected to each other or to the logic blocks. In order to connect the pieces to each other, programmable switches are used. The pieces could have different lengths. Input/output blocks are applied for FPGA pins in different modes and also for different voltages of 3.3 or 5 volt. Designing input and output blocks should be so that they could implement different logic circuits on FPGA. Usually, there is an inverse relation between complexity and flexibility of logic blocks and connection resource. It means that increase of one of them leads to decrease of the other one and vice versa[7].

Linear clustering: Clustering refers to including a set of objects in a group. In this case, objects located in similar clusters are similar to each other. Choosing algorithm of the proper clustering and collection of parameters are dependent on unique sets and exploiting results.

In order to assure one that a linear relation is available in the paired images of clusters; one clustering algorithm has been presented. Clustering algorithm is able to decrease complexity of the relation training process. Block diagram indicates stages applied to the clustering algorithm.

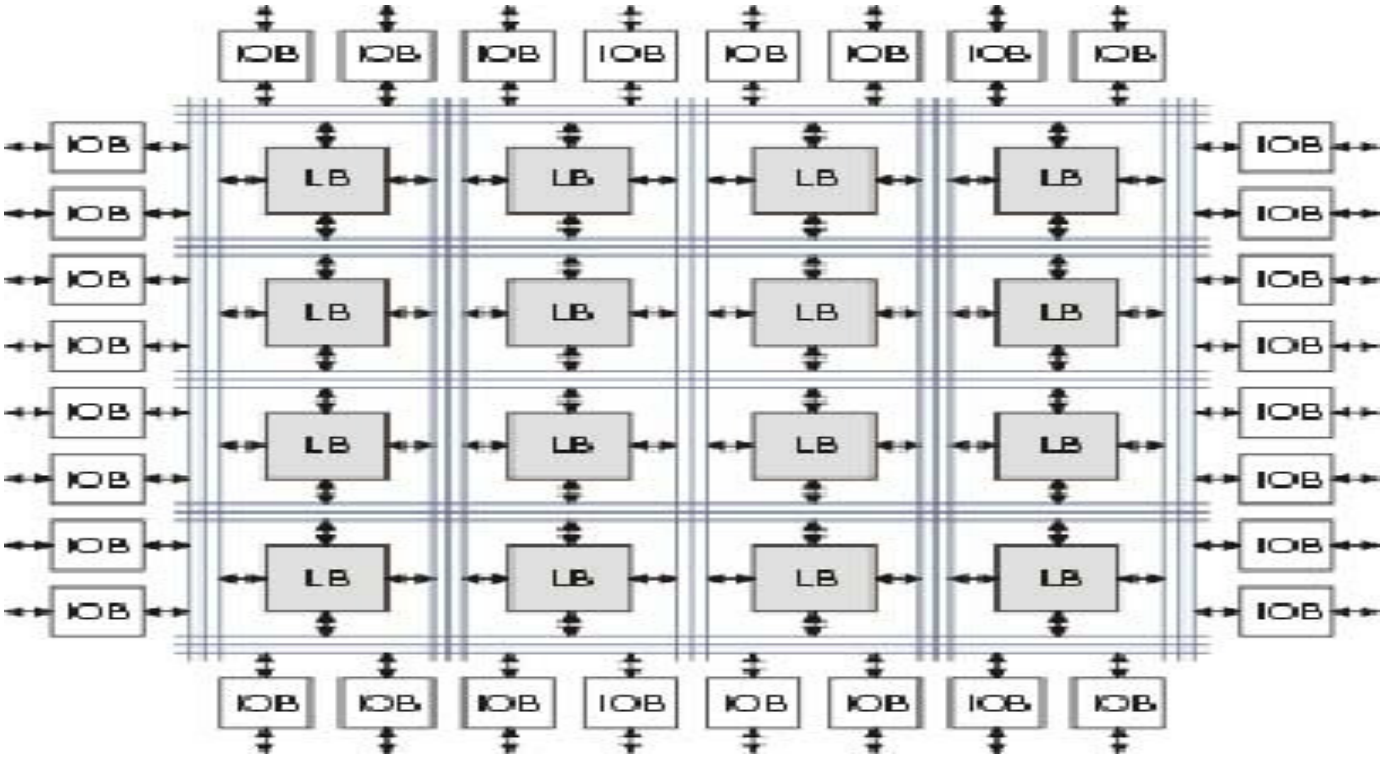

Figure-4
The overall structure of FPGA

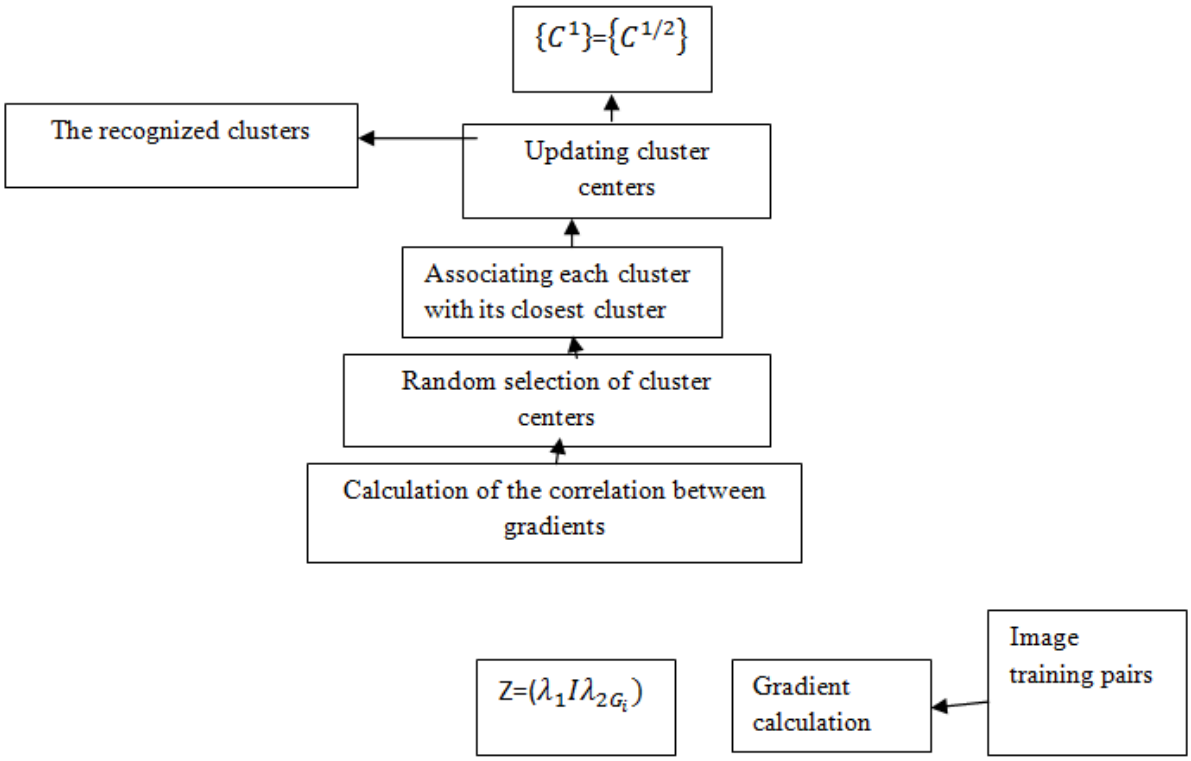

Figure-5
Block diagram of clustering algorithm

Two parameters are used in the clustering algorithm: Gradient of low-resolution image, Low- resolution image.

Results and Discussion

Results of simulation: The models are designed based on Verilog software and simulated by the model of Sim 6.3g. Figure 6 indicates clustering simulation results based on available data and linear relation in RAM that indicates input and output of visual data via simulation.

FPGA implementation long range transceiver module is combined in XILINX ISE 9.2 i based on Sim 6.3 g software and is programmed in the existing XILINM Vitex5. Different executive levels such as synthesis, image implementing, and observing RTL information related to routing, placing, and programming have been defined and presented as follows:

Synthesis and implementing the image: Table-1 indicates a summary of synthesis and image implementing with regard to the long range transceiver module. The table 1 shows that total number of gates needed for this design equals 2316547 gates. Therefore, the table shows that it is possible to gain information via FPGA software[8].

Transistor resistance logic imaging makes one aware of the diagram of the pin related to the long range transceiver module. The required data for suitable placing in the production level will be revealed with regard to the report of routing and placing and via FPGA. According to FPGA, a single time co-ordination of central processing with the real time environment is obtained[9].

Conclusion

Over the recent years, image processing has significantly been developed both theoretically and practically. Today, presence of image processing is observed in many of the sciences and industries. Image processing has affected fourteen different fields including medical industry, military and security sciences, geology, astronautics and astronomy, urbanization, art and cinema, scientific technologies, politics and psychology, architecture, economy and advertising, meteorology, archeology. Some of these applications are so dependent on the image processing that they are out of use without it. Though it is impossible to mention all details of image processing applications in this paper, the problem related to low- resolution face recognition has been discussed. In order to have an image with high- resolution, a new data limit appropriate for testing error in high-resolution image space has been provided and RLSR has also been presented. Empirical results indicate the number of clusters in the algorithm. The achieved results have been useful. Moreover, the results show that the relation resulted from mean of relations in each cluster requires less time via decreasing retrieving error.

Table-1
A summary of synthesis and implementing the image

Number of BlockRAM/FIFO	16	32	50%	
Number using BlockRAM only	16			
Total primitives used				
Number of 36k BlockRAM used	16			
Total Memory used (KB)	576	1,152	50%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Total equivalent gate count for design	2,316,547			
Additional JTAG gate count for IOBs	2,448			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Thu Nov 15 12:03:51 2012	0	329 Warnings	49 Infos
Translation Report	Current	Thu Nov 15 12:03:55 2012	0	0	0
Map Report	Current	Thu Nov 15 12:05:15 2012	0	3 Warnings	7 Infos
Place and Route Report	Current	Thu Nov 15 12:05:44 2012	0	0	3 Infos
Static Timing Report	Current	Thu Nov 15 12:05:54 2012	0	0	3 Infos
Bitgen Report					

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