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# Survey on Multi Field Packet Classification Techniques

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## Abstract

*The latest research frontier on next-generation routers targets at more integration of advanced networking capabilities and functions including firewall operations, memory access control, quality of service (QoS) management, policy routing, and traffic billing. To realize such services, the router should be able to categorize the packets into different flows depending on already defined rule set called classifier, which contains a range of values of different fields in the packet header. The stated functions are defined as multi field classification. The increase in link rate and the size of classifier creates the challenge in multi field packet classification in the design of faster routers. We present a survey on various algorithms and architectures proposed for multi field packet classification that achieves higher throughput.*

**Keywords:** Packet classification, routers, rules, FPGA.

## Introduction

The need to maintain the security and efficiency of network operations has become inevitable in the light of the increased in the rate of internet expansion. Network services such as intrusion detection, management of traffic, and access control based on their multi-field headers, discrimination of network packets are required. In addition, advance packet classifiers are needed to cope with internet applications that are emerging.

The set of rules or classifier used by the routers are based on the fields of packet header such as type of protocol, addresses of source/destination, and port number source/destination. The set of rules are associated with an action to apply to packet that matches the pattern rule. Network virtualization recently emerged as a feature that is essential for next generation networks, cloud computing, and data center; and this has placed the requirement of flexibility and provision of clean interface per control plane upon the underlying data plane[1].

For the implementation of packet classification functions, identification of information of incoming packet is necessary for the routers. Each of these packets have specific classifier in which set of rules used for header field values checking are contained. The process by which the rules in a classifier identifies that the incoming packet matches is called packet classification. The classifier s rules consist of the following: an action value and five fields which are protocol number, source port, source IP address, destination port, and destination IP address. The matching rule in the classifier is searched by the router to decide an action to be taken for incoming packet.

To resolve the problem of multiple matching, a priority value is assigned to each rule and the router executes the action corresponding to so called best matching rule that has the highest priority.

In this paper we give the basic ideas on multi field packet classification in section 1. Section 2 surveys the existing techniques, algorithms and discusses their limitations. Comparison of the most important FPGA designs in section 3. Section 4 is the conclusion.

## Multi Field Packet Classification

Firewall devices, traffic billing, QoS etc. are various applications in a network that requires multi field packet classification. Generally, multiple-field packet classification is not an easy problem. The categorization of packets into different flows are done by flow classifier which contains the set of rules. Packet classification requires that every packet is compared with the predefined database of rules and applying the action on the packet based on the rule of highest priority.

Currently the order is increased for routers to supply QoS to various applications, hence the routers require new capabilities such as reservation of resources, per-flow queuing, admission control, and others. Distinguishing of packets of different flows is requirement for the router by the aforementioned mechanisms.

As shown in figure 1 the instructions about the information carried by the packet are contained in its header, which include synchronization, length of packet, packet number, originating address, destination address, protocol, and port numbers of source/destination are used to find the matching rules in the database.

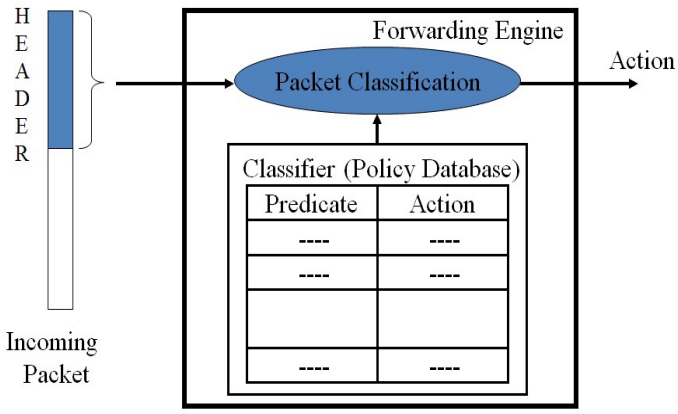


**Figure-1**
**Packet classification[2]**

The database contains rule set labeled as R1, R2, R3…, RN where these rules are stored in a certain sequence and each rule consist of d values. Each field of the rule undergoes three types of matches[3]:

Exact match: where values of header field should be identical to the value of the rule filed. The exact match is used for protocol such as TCP and UDP.

Prefix match: The rule field should be a prefix of the header field where the prefix match is represented by using values followed by * wildcard. If the wildcard * occurred alone without values this means any value can be matched to this field.

Range match: The values of packet header fields are within a particular range defined by the rule. This is exploited for ranges of port number.

The packet matches the rule only if each packet field matches the corresponding rule field. Additionally, each rule in the classifier includes action which defines the process to be applied to the packet matching the rule.

A tuple is basically the field in the header of a packet. 5 tuple[4] is a term used in computer networks to refer to a set of five different values that make up a Transmission Control Protocol/Internet Protocol (TCP/IP) connection. The tuple is employed by network and system administrators in identifying the key requirements to create an operational, secure and bidirectional network connection between two or more local and remote machines.12 tuple are used in next generation packet classifications. The primary components of 12 tuple are the ingress port (router port number determine the ingress port width, as an example router with port number equal to 63 means it has 6 bit ingress port), address of Ethernet Source/Destination, type of Ethernet, ID of VLAN, priority of VLAN, address of IP Source/Destination, IP type of service bits, and port number of source and destination. An example rule set for 12-tuples for classifying the packets is shown in table-1.

Multi-field packet classification requires high throughput along with maximum utilization of memory. For example, the cutting edge link rate has been pushed to 40Gbps, requiring that a packet is processed at the rate of 8 ns in the worst case (for packet having a size of 40 bytes minimum). Achieving such processing using available software processing method is not realistic. Therefore, finding new techniques to enhance the processing speed is popular research activity.

## History of Multi Field Packet Classification

The research in the field of packet classification falls into two categories algorithmic based and hardware based solutions. The algorithms on packet classification have been in the near passed a subject of thoroughly researched. Packet classification schemes based on software have been proposed by Chao[5]. However, the performance requirement by internet backbone routers in term of speed cannot be attained through software processing. The approach of special hardware support is an attractive alternative to enhance the speed of search. The following section analyzes the important researches and techniques carried on multi field packet classification. The section includes survey of not only the earlier works but also includes most recently carried researches as well.

**Table-1**
**Example of 12-tuple rule set**

| Rule | Ingr port | Eth scr | Eth dst | Eth type | VLAN ID | VLAN priority | IP scr (SA) | IP dst (DA) | IP protocol | IP ToS | Port scr (SP) | Port dst (DP) | Action |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R1 | * | 00:13 | 00:06 | * | * | * | * | * | * | * | * | * | Act0 |
| R2 | * | 00:07 | 00:10 | * | * | * | * | * | * | * | * | * | Act0 |
| R3 | * | * | 00:0F | * | * | * | * | * | * | * | * | * | Act1 |
| R4 | * | 00:1F | * | 0×8100 | 100 | 5 | * | * | * | * | * | * | Act1 |
| R5 | * | * | * | 0×0800 | * | * | * | 01* | * | * | * | * | Act2 |
| R6 | * | * | * | 0×0800 | * | * | 001* | 11* | TCP | * | 10 | 15 | Act0 |
| R7 | * | * | * | 0×0800 | * | * | 001* | 11* | UDP | * | 2 | 11 | Act3 |
| R8 | * | * | * | 0×0800 | * | * | 100* | 110* | * | * | 5 | 6 | Act1 |
| R9 | 5 | 00:FF | 00:00 | 0×0800 | 4095 | 7 | 0011* | 1100* | TCP | 0 | 2 | 5 | Act0 |
| R10 | 1 | 00:1F | 00:2A | 0×0800 | 4095 | 7 | 01000001 | 10100011 | TCP | 0 | 2 | 7 | Act0 |

**Algorithms Based Techniques:** Algorithms for packet classification use two operations which are preprocessing and classification. In preprocessing an optimized data architecture is built which exploits the dependency characteristic existing among rule set. For every packet the generated data architecture is used to find the best matching rule. Preprocessing operation is needed only if the classifier is updated by adding, deleting or modification of rules.

The classification operation uses the packet header to search the data architecture built in the preprocessing operation in order to find the least cost rule. This operation falls to data plane of network operations which make the processing speed of this stage very critical[3].

The Taylor[6] classifies algorithms of packet classification into four categories. Figure 2 outlines these categories.

**Exhaustive Search Category:** Linear search and TCAM falls in this category where in linear search the rules are stored in database in decreasing priority where the search process is performed by comparing the incoming packet with all database sequentially to find the matching rule. The advantage of linear search is the memory efficiency where the required storage is O (N) where N is the number of rules in the classifier but the drawback is poor scalability for big classifier because linear search needs O(N) memory accesses for every packet classification[7].

Decomposition Category: Decomposition based methods perform independent search on each field and finally combine the search results from all fields. Such algorithms are desirable for hardware implementation due to their parallel search on multiple fields.

Pankaj and Nick[8] introduce Recursive Flow Classification (RFC) algorithm that exploit the advantage of classifier which found to contain considerable redundancy. In RFC S bit in the packet header is mapped to T bit of classID where (T ≪S) using real classifier rules. In the RFC algorithm when hardware pipeline is used 30 M packets per second can be classified. However, when software is used 1 M packets per second are classified.

Bit vector algorithms originally proposed in BV[9] and enhanced by Baboescu F. et. al.[10] present the aggregated bit-vector algorithm (ABV) which added two ideas recursive aggregation of bit and rearrangement of filter in order to reduce memory accesses. The assumption the algorithm based on that the packet in real life rule set matched small number of rules. Memory access has been reduced where for every X bit exist in the original bit vector an aggregation bit is recursively generated. It is necessary to examine the bit map values if the aggregation bit is set. Rearranging multiple filters which match a specific packet close to each other increased in the reduction of memory access is achievable. By this way, the same aggregation group contains the multiple matching rule sets. However, more reduction in memory result as filter wildcard increased. Additionally, deficiencies of tree using include increase in memory usage as a result of classification inefficiency and variation of time required for classification which depends on the value of income packet-this changes the path inside the tree.

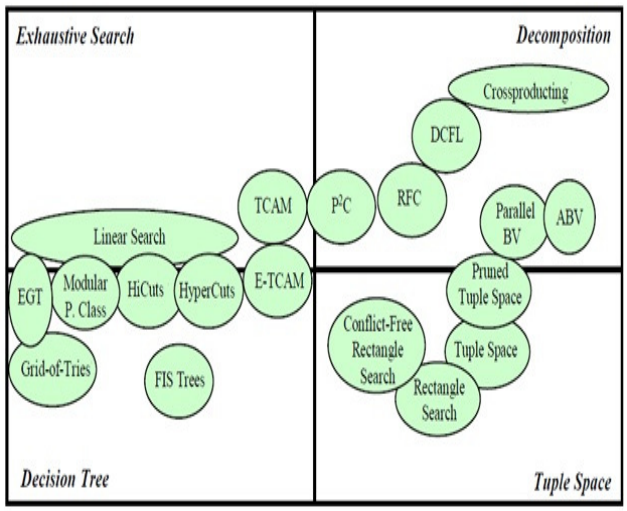


**Figure-2**
**Categories of packet classifications techniques**

Taylor[11] et al. introduced a decomposition-based algorithm known as Distributed Cross producing of Field Labels (DCFL) in which feature of the classifier is exploited. Problem of multi field searching were decomposed and search engines that are independent were utilized, these work in parallel in searching the matching rule for each filter field. DCFL by employing Bloom filters and intermediate search results encoding uses a network aggregation nodes in the place of bit vectors. The algorithm avoids the exponential increase in the time or space required during the execution of this operation in a single step. The authors predict that in the implementation of DCFL that is optimized, over 100 million packets/second can handled and 200,000 and above rules can be stored in the most recent FPGA devices or application-specific integrated circuit (ASIC) without the need of external memories.

DCFL algorithms have two major phases, in the first phase each field of packet is independently searched and the results from this phase are combined in the second phase. The fundamental challenge in performing this technique is in the second phase that means how the searches results of single field combined efficiently.

However, to get the final result intrinsic storage usually required for merging the results of independent search. Algorithms that are decomposition based suffer from poor scalability, and suitability only for small classifier.

Decision Tree Category: A decision-tree-based algorithm for

packet classification has made good progress mainly because it can be implemented using pipelining architecture. There are several algorithms which solve the classification problem based on geometry partitioning of the rule set. The number of header fields D in a dimensional space in the rule represents a hypercube where every packet specifies a point in the D dimensional space. A small number of heuristics are employed in the building of decision tree algorithms so as to divide repeatedly the space into sub spaces with fewer rules; which enhances low cost linear search in finding matching rule that is optimum. Building the decision tree makes easy that algorithm to look up the packet. The value of packet header is used by the algorithm to find the destination subspace in which linear search is performed to find the matching rules.

In 2000, Hierarchical Intelligent Cuttings (HiCuts) algorithm was introduced[12]. It had been a popular decision tree based packet method in which decision tree is built based on local optimization decisions at each node in order to decide which dimension to cut and the number of cuts to be made.

In 2003, HyperCuts[13] algorithm was introduced as an enhanced version of HiCuts, where per step cutting is done on multiple fields. As a result decision tree that are fatter and shorter are realized.

Explicit range search was proposed by Luo[14] in 2008. This method enables more cuts per node in comparison to HyperCuts. There is a tradeoff of the height of tree at the expense of increased memory consumption. Different number of access to memory may be required at each internal node to decide traversing with child node, this requirement renders pipelining infeasible.

In 2010, EffiCuts[15] algorithm was proposed to eliminate overlap among small and large rules. The researchers separated all small and large rules. In this approach, they defined rules subset to be separable if all the rules in each dimension are either large or small. For each subset a distinct tree is developed where to separate the large rules each dimension can be cut, or finely the small rules are separated without incurring replication.

In 2013, Boundary Cutting[16] based packet classification algorithm was proposed. This algorithm finds out the space that each rule covers and performs the cutting according to the space boundary. Thus, the cutting in the proposed algorithm is deterministic rather than involving the complicated heuristics, and it is more effective in offering improved search performance and more efficient memory requirement.

In general, decision tree algorithms become attractive solution targeting big size classifier because they provide better trade off between memory and speed.

Tuple Space Category: Tuple Space is a generic packet classification algorithm. The main idea that the real databases typically use only a small number of distinct field lengths and mapping filters to tuples where the number of tuples in comparison with the rule number in the filter is much less as a result even a simple linear search of the tuple space can provide significant speedup over native linear search over the filters. Each tuple is maintained as a hash table that can be searched in one memory access. Tuple Space introduces techniques for further refining the search of the tuple space, and demonstrates their effectiveness on some firewall databases. In real database since the number of tuples can be very large and lookup throughput performance suffers the tuple pruning[17] technique is developed to reduce the number of tuples that has to be searched during the lookups. The observation is for any given packet, the number of unique prefixes matched on a particular field is typically small. So if we could perform the longest prefix match first on some field and figure out the lengths of the matched prefixes, then only a subset of tuple groups need to be searched[6].

Tuple Space is suitable for multiple fields. It has fast average classification and update time. However, classification is non-deterministic and classification time is long. Tuple Space Search is a classic algorithm for multi-dimensional packet classification but when the number of tuples is large, its performance degraded singnificantly[18].

Limitation of algorithms come mainly from that performance evaluation of algorithms is based on the assumptions and features of filters in reality where these algorithms are targeting certain classifier and work efficiently only on this classifier. Additionally, algorithms need big memory access resulting in low speed processing.

Taking into consideration these limitations these algorithms not expected to work efficiently in the case of increased requirement for bigger classifier especially for next generation routers.

**Ternary Content Addressable Memory (TCAM)**: Because of the inherent advantage of straightforward design, speed and good management associative with TCAM, it has become the choice method for determination of problem of packet classification. In this method all rules are checked at the same time using parallel hardware. Search operation in TCAM involves the input data comparing with all TCAM contents and the result appear in one clock cycle. Over the past few years TCAM as device for subject been investigated by many. Fundamental issue considered has been that of the improvement of TCAM range representation space efficiency.

Shah and Gupta[19] optimize update on TCAM by proposing two algorithms. First, The Prefix-Length Ordering Constraint algorithm (PLO-OPT) where the main idea is to keep all the unused entries in the center of TCAM. Comparing the PLO-OPT to previous works it found that it decrease the time required for update by a rate of two. Secondly, The Chain-

Ancestor Ordering Constraint Algorithm (CAO-OPT) offers 1.02 - 1.06 memory accesses per update.

Liu H.[20] propose two methods targeting reducing the size of forwarding table and optimizing TCAM resource usage. The two methods are pruning and mask extension where the pruning is used to remove redundant routing prefix then the mask method used to mask extension to further reduce table size. The author claims that using both techniques achieves up to 45% compaction ratio.

Efficient Mapping of Range Classifier into Ternary-CAM[21] proposed a novel scheme to get efficiently mapped ranges into TCAM. This proved that TCAM as a low cost commodity hardware which can be used for high speed deterministic classifications.

To handle the power consumption problem in large TCAM, the Panigrahy R. and Sharma S.[22] the forwarded table is partitioned equally using prefix ranges and put each part into different block of TCAM. The IP address is examined by a set of range comparator and decides the TCAM block to activate to enable search the IP address. The forwarding engine with K way partition will reduce TCAM power consumption K times. The implementation of such TCAM can be found in liturature[23].

A fast and scalable packet classification using TCAM was proposed in P2C[24]. Key features of this proposed scheme is its ability to conform with classification of rule set complexity, and the requirement for storage and dynamic updates can be tuned at the granularity of individual rules.

Extended TCAM introduced by Spitznagel E. et. al.[25], which implemented in hardware the range matching directly and also reduces the usage of power by over 90% in comparison to standard TCAM.

The researcher[26] present a novel architecture called BV-TCAM in which multiple matches in Gbps are reported. TCAM perform the look up of header fields which can be a prefix or exact value, while the tree-bitmap is used to implement source and destination port look up. The actual implementation on FPGA is not reported but they claims that the consumption of circuit is lower than 10% of the logic and less than 20% of the RAM block with 222 rules and they claim that if the design implemented on advanced FPGA by exploiting pipeline throughput of 10 Gbps can be achieved.

Another research[27] published as algorithms for advanced packet classification with ternary CAMs introduced two different algorithms to address two important problems that are encountered while using TCAMs: reducing range expansion and multi-match classification.

In recent years, few Gray code based[28] and focusing on low power and High speed[29,30] TCAM approaches are also introduced for packet classification.
The major concerns with TCAMs are its storage inefficiency of range data that makes TCAM got low memory capacity which may not be sufficient in next generation IP networks and it requires high power to classify the packet. TCAMs have significant disadvantages in terms of clock rate, power consumption, and circuit area.

**FPGA based Technique:** Field-programmable gate arrays (FPGAs) combines the pros of software and hardware. FPGA provide huge resources and better performance than software and can be programmed easily to provide a wide range of applications. Because FPGA offers massive parallelism and reconfiguribilty FPGA becomes increasingly popular in the field of network processing[3, 4].

The main purpose of developing FPGA for packet classification is to accelerate the existing algorithms where the design should be able to receive the packets, processes the packets, and forwards the packet with wire speed while utilizing the maximum network bandwidth.

Although multi-dimensional packet classification is a saturated area of research, little work has been done using FPGAs where most work focusing on 5 tuple using decomposition and decision tree algorithms. In this section the most important multi field designs are discussed followed by comparative analysis.

Distributed Crossproducting of Field Labels (DCFL)[31,32] extension was presented and produce a hardware implementation which is reconfigurable and this device is an extension of TCAM (ETCAM). Xilinx Virtex 2 is the target FPGA device for implementation. Due to the technique based on memory intensive on fly updating remained feasible. 50 million packets per second were achieved with 128 sample rules. The authors claim that if the design implemented on Virtex 5 FPGA throughput of 24 Gbps can be achieved.

Kennedy A. et. al.[33] proposed an architecture that is low power for high speed router. In this work the matching of oscillations in traffic on router line card by employing dynamic changes in clock speed of an energy efficient packet classifier was achieved by adaptive clocking unit. In this architecture 40 Gbps line speed is achievable with 49000 rules and in addition 17.88 power saving is achievable when the architecture is implemented on Cyclone 3 , Stratix 3 FPGA and ASIC.

Architecture[34] describe a Dual Stage Bloom Filter Classification Engine (2sBFCE) which is memory efficient classification based on FPGA targeting a 5 dimensional classification with 4k rules and employing 128 k bytes of memory. The design needs an average of 26 clock cycles for packet classifying with over 6 Gbps throughput or 2 Gbps on an average condition and worst case respectively.

Features of recent FPGA and algorithms of decision tree based

were exploited by Jiang W. et. al.[35]. HyperCut algorithm is used due to its scalability feature in form of multi field packet classification in FPGA. Two dimensional dual pipeline architecture for a decision tree based algorithms targeting multi field packet classification has been proposed. Rule replication problem reduced by proposing two techniques named precise range cutting and rule overlap reduction. The results show that the design can support 10 K rules using Xilinx Vertex 5 FPGA on chip memory with throughput of 80000 Mbps for minimum packet size of 40 bytes. The authors claim that this is the first design that can support 10 K rules using FPGA.

Puš V.et. al.[36] describe a novel algorithm which is problem decomposition based using perfect hash function targeting for high speed networks. The three basic steps in packet classification are Longest Prefix Match (LMP) operation, The LMP results mapping to the rule number (this is achieved using packet hash function in order to perform fast searching), and the checking of packets against the resulting rules (this is necessary because mapping of packets to some rule number is done by the hash function even if the packet does not match any rule). As a result, in the third step the rule table has to be stored. A unique feature of the algorithm is access to the external memory with constant time complexity. By using FPGA and a single SRAM chip of 150 MPPS throughput can be achieved.

A novel design based on the advantage of a very compressed version of Deterministic Finite Automata (DFA) was presented by Antichi G.et. al.[37]. The architecture was implemented on NetFPGA to classify packet at line rate. However, the architecture was not evaluated using any known benchmarks and did not report the preprocessing time.

The Pipeline architecture presented by Chang Y.K. et. al.[38] is called Set Pruning Multi-Bit Trie (SPMT). The problem of rule duplication is reduced by two techniques. First, partition by wildcard (PW) which divide the rules into sub groups based on the wildcard field position. Secondly, the rules are partition into subgroups in partition by length rule based the lengths of prefix. The architecture implemented on Xilinx Virtex 5 FPGA with throughput of over 100 Gbps and supports 10K rules on chip memory.

The recently proposed Open Flow switch[39] flexibility and programmability is brought to infrastructure of network and network virtualization is also enabled. OpenFlow is an effort which manages the network flow explicitly by means of rule set with rich definition such as the interface of software and hardware. About 12-tuple fields are considered[4] in OpenFlow which is also referred to as coming generation packet problems[40].

Recent architecture targeting for Openflow is presented by Jiang W.et. al.[40]. The architecture is a novel design tree based linear algorithm and packet classified using 12 tuple header field. The design uses the parallelism provided by current FPGA to propose two dimension multi pipeline architecture. 10000 5-tuple rules or 1000 12 tuple rules with performance of 40 Gbps (throughput) for size of 40 bytes minimum packet has been achieved. However, the architecture evaluated based only on the ACL benchmark from ClassBench.

Another work targeting Openflow like 11 tuple reported by Fong J.et. al.[41]. The authors propose ParaSplit algorithm for memory requirement reduction and optimize the partitioning using the technique of Simulated Annealing. The architecture implemented on FPGA and by exploiting the parallelism high throughput is achieved.

The Ohlendorf R. et. al.[42] proposed a new technique for packet classification aimed for implementation on chip within a network processor. The main focus of the algorithm is the provision of QoS for thousands of flows by means of multi field packet classification. Incoming packets are assigned to different processing paths within the network processor using the classification algorithm. Also, the authors present the outlines for FPGA prototype implementation.

Another hardware approaches that has been proposed are dedicated RTL[43-45]. The Papaefstathiou I. et.al.[43] proposed an architecture that is SRAM based which is Dual port IP Lookup (DuPI).

**Table- 2**
**Comparison of different packet classification methods with important parameters**

| S.No | Technique | No. of rules | Memory Utilized | Area | Throughput | Max.frequency(Mhz) |
|---|---|---|---|---|---|---|
| 1. | Optimized HyperCuts | 9603 | 612 | 79% | 80.23gbps | 93.77 |
| 2. | Simplified HyperCuts | 10000 | 286 | 89% | 10.84gbps | 84.89 |
| 3. | BV-CAM | 222 | 16 | 8% | 10gbps | 120.34 |
| 4. | 2sBFCE | 4000 | 178 | 53% | 2.06gbps | 102.66 |
| 5. | DCFL | 128 | 221 | 8% | 24gbps | 157.09 |
| 6. | openFlow | 9603 | 432 | 74% | 91.73gbps | 100.50 |
| 7. | Improved HyperCuts | 10k | 407 | 33% | 80.23gbps | 125.4 |
| 8. | PW | 5k | 263 | 8% | 107.16gbps | 167.44 |
| 9. | PW PL | 10k | 429 | 24% | 110.73gbps | 173.02 |

The major limitations in the current FPGA designs they uses big amount of resources inside FPGA and the power usage is not reported clearly.

## Comparative Analysis

Table 2 compare the performance of few recently proposed hardware based packet classification techniques based on their memory utilization with area, throughput and the maximum frequency. For justifiable benchmarking previous work used were scaled to Xilinx Vertex 5 platforms with maximum clock frequency. The comparison results show that the decision-tree-based methods are achieving high throughput with lower area and also maximum frequency.

## Conclusion

This paper presents detailed study on important research works carried on multi field packet classification. The proposed algorithms failed to fully provide the requirement of network devices. Theoretical bounds show that it is difficult to achieve both high classification rate and modest storage in the worst case. As already stated in many researches, TCAMs in comparison to SRAM cannot change in scale with respect to speed of operation, power usage, and size of circuit. Also, solution based on TCAMS in the process of converting ranges into prefixes is affected by range expansion.

Overall study shows that mapping packet classification algorithms onto hardware based pipeline architectures appears to be a promising alternative in future for packet classification. In algorithms based on decision tree classification of a packet is done by tree traversing where a throughput of a packet per clock cycle is realizable when algorithms are properly pipelined. As studied from the comparison results we can observe that the decision-tree-based methods are achieving high throughput with lower area and also maximum frequency. However, algorithms based on decision tree classify packet with aid of a number of memory access that can be varied.

In the next-generation packet router when considering the classification of packets which have more than 5 tuple packet header; the future works should focus more on optimization techniques. Packet classification algorithms that are based on decision tree must be improved with reduction in memory, such that into single FPGA 10000 5 tuple or 1000 12 tuple of rules can fit easily. The emerging on chip processing requires meeting these problems with lower power and high performance too.

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