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Design of Low-Latency 4K HEVC using V-By-One HS Transmission

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Abstract

High Efficiency Video Coding (HEVC) is an advanced video coding technique, which is designed to double the Data compression ratio compared to the other video standard with the same level of video quality. The HEVC video coding layer uses the same hybrid approach used in all modern video standards used in earlier H.264. To achieve the high compression ration HEVC supports the recursive quad-tree coding unit structure and 64 × 64 coding tree unit. These features require inter/intra-picture prediction and 2D transforms coding. These are transmitted through the v-by-one HS and new structures of read controller for memory and a sum of absolute difference (SAD) summation block was designed. The memory read controller was designed to reduce the internal memory read time, and the SAD summation block structure supports the recursive quad-tree coding unit structure and the asymmetric motion partitioning mode. Based on requirements of higher-resolution and more color-depth the pixel data problems are transmitted through v-by-one HS by increasing data rate. Here the number of transmission medium will be reduced to solve the skew problem, power consumption and Electromagnetic interference.

Keywords: High Efficiency Video Coding (HEVC), H.264, Advanced video coding (AVC), Joint Collaborative Team on Video Coding (JCT-VC), Moving Picture Experts Group (MPEG), MPEG-4, standards, Video Coding Experts Group (VCEG), video compression..

Introduction

The High Efficiency Video Coding (HEVC) design is the very recent joint video project standard of the ITU-T Video Coding Experts Group (VCEG) and the ISO/IEC Moving Picture Experts Group (MPEG) standard organizations with Video Coding (JCT-VC)[1]. From the recent trends HEVC was designed to overcome the existing video resolution and increase the parallel processing architecture by essentially designing with existing H.264/MPEG-4 AVC video applications. High video resolution was achieved by increasing the reusability and standardizing the bit stream constraints with decoding structure. This standard will provide the maximum space to optimize the compression ratio with low cost. HEVC encoder first proceeds by splitting a picture into macro block and the intra-prediction random access point in the first picture. An intra-picture prediction will be performed when the prediction of the blocks in the picture is based only on the information in that picture. After the completion of the prediction method the picture goes through v-by-one HS to final picture representation and is stored in the decoded picture buffer for further identification. The decoded picture from the buffer will be used for next picture prediction. The High Efficiency Video Coding is performed by compressing higher ratio using the basic unit size of 64x64 called Coding Tree Unit (CTU) and the Asymmetric partitioning mode[2,3]. These features provide more flexible in prediction of size than the previous standards. But previous motion estimator system does not support these features[4,5]. HEVC technology is designed for digital video applications in all video application which are not covered in previous applications like H.264. These features are used in all video applications like HDTV and other video processing systems. These transmissions are done through the V-By-One HS, which is much faster than the previous transmission applications.

V-By-One HS is an high speed electrical signal standard which can run faster over twisted pair copper cable. It is designed to transmit the pixel data with high resolution and expansion in color depth by removing the interface between the cables. V-By-One HS is a latest standard which uses CDR and Equalizer, that achieves 3.75 Gbps by removing Skew problems, EMI and power consumption. Equalizer of V-By-One HS improves the quality of data transmission by enabling the data transmission expansion for longer distances.

Design of HEVC Coding

The main aim of HEVC coding standard is highest coding efficiency. This coding efficiency includes transport system integration with lowest possible bit-rate without any loss of data. From the above two standard coding efficiency of the HEVC standard is measured. These parameters are defined from the Coding Tree Unit (CTU) sizes, which are encoded by progressively smaller CTU sizes. The more details associated with decoding blocks are explained below.

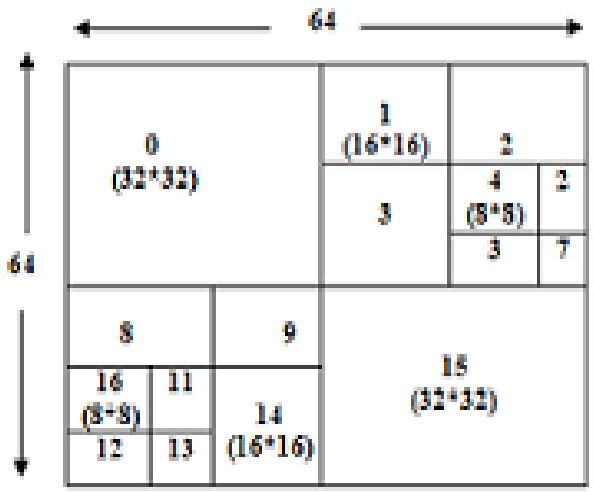

Figure-1
Picture partitioning

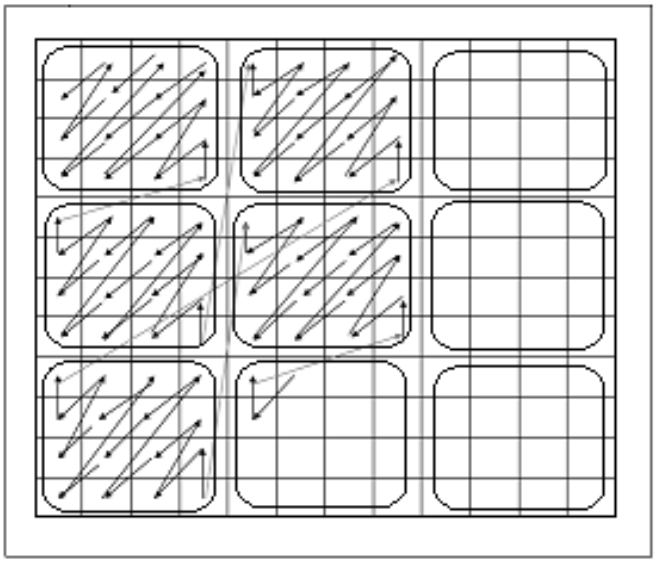

Figure-2
Luma Interpolation Scanning

HEVC Partition Structure: HEVC system consists of Memories, Processing elements (PE) and Sum of Absolute difference (SAD). These memories used to save the reference frame and Coding Tree Unit. From the pixel values of the reference frame the SAD values are calculated by the PE for the next frame. In HEVC, pictures in CTB are spitted recursively into quad-tree structure which will appear in raster order depending on the stream parameters (figure 1), all the way down to zero also called coding units (CU). The bit rate was increased for all test sequences by 64x64 CTU sizes compare with 32x32 CTU, all the way down to 8x8. These test results shows that coding efficiency was increased for large CTU compare with small CTU size. In HEVC sequence of CTB is called as slice and each slice are split up into slice segments which allows the low latency of transmission without any coding efficiency loss. These are transmitted over the V-By-One HS which transfers at 3.75 Gbps to achieve 4K resolution. Throughout these entire revolution the evolution have been made to maximize the compression capability without any loss of data.

HEVC Video Code Scanning: Like previous compression standards HEVC also performs same hybrid approach like Intra/Inter prediction and 2D transform coding. In first HEVC encoder splits the picture into block shaped region which uses intra picture prediction. Intra-picture prediction is performed in the blocks of the picture based only information in the same picture, otherwise inter-picture prediction is performed. Commonly in HEVC encoder intra-picture will be performed for the first frame of the picture and for the next frame of the picture inter-picture will be performed. For each prediction HEVC is performed by residual coding. It supports four transform sizes 4x4, 8x8, 16x16 and 32x32 and these theses transforms are based on the Discrete Cosine Transform (DCT) which uses the coefficient of 7 bit storage. From the above transform High precision and Large size of Transform are performed to achieve HEVC when compare with AVC.

The residual signal consist of one or more transform unit, which is recursively split up with the same quad tree method with smallest allowable block of 4x4. For example 16x16 could split-up into three 8x8 and four 4x4. So the least one in the CU is 4x4 Luma. If the TU has the size 4x4 the transform will simply bypass all together which is called transform skip and transmit inverse quantization through V-By-One HS. In this way TU coefficients are coded in the bit stream which is differ from the AVC. In residual coding first bit stream signals are the last position, which indicates position of the last coefficient in scan order. From the above, the decoder starts scan backward from the last position until it reaches 0,0. The coefficients are arranged in group, each group and each coefficient in the group are scanned diagonally (from down and left) as shown in figure 2. The root of the HEVC is Coding Tree Unit (CTU). In HEVC pictures are partitioned into Coding Tree Blocks (CTB) instead of macro blocks. HEVC decoder decodes all the non-zero coefficients in the group and it continues until reaches zero coefficients, and it moves to the next group. By this all the sign bit coefficients in the group are coded. In HEVC there is an option called sign bit hiding if enabled one of the sign-bit in the group is not coded, but rather inferred. The inferred missing sign will be equal to the least bit of the sum of all the coefficients absolute values. This was the option to the encoder coding to adjust one of the coefficients up or down to fix inferred sign.

Memory Controller: The figure 2 shows the scan order process of the picture, which calculates the search area immediately. In search area memories are placed in each line, it calculates only one area for each clock cycle. There is no problem in the direction of scan order, but there is a restriction while scanning. The line memory of the last search area should read 64bit in one clock cycle. If memory increases the memory read operation will increase which creates unnecessary clock cycle in one 4K-

HEVC frame. To overcome this problem extra registers will be added at the bottom line of the memory as shown in figure 3. In the figure 3 dotted lines shows the one direction of the search order and the dashes line shows the remaining direction of the search order. The added registers are shown in the bottom line which reduces the usage of clock cycle.

Quantization and Deblocking: HEVC uses uniform reconstruction quantization (URQ) to transform various block size which supports Quantization Scaling matrices. Context Adaptive Binary Arithmetic Coding (CABAC) is used for its compression performance and to reduce the memory requirements. Deblocking is used for inter picture prediction block by filtering prediction block. But using this Deblocking method the design process is simplified by its decision making and filtering process. Here non linear mapping is designed within inter picture prediction by mapping its amplitude. The main aim of the mapping is to reconstruct the original amplitude using the look-up table which is described by additional parameters at the encoder side.

Intra/Inter Picture Prediction: Intra/ Inter picture of the frame was performed by Prediction units and prediction block. The CU have the 8 partition modes from the mnemonics as shown in figure 4, and N represents the half the length of CU and u represents the one quarter. Thus CU consists of one, two or four prediction unit. CUs are split-up into PU, whether the area is intra-coded or inter-coded. The decision of a code is, which area should perform a intra picture prediction and which area should perform a inter picture prediction at the CU level. Because the heart of the prediction unit at CU level only. Depending on the basic prediction type the decision should be taken, whether Luma CB further split-up into prediction blocks. HEVC supports prediction block size from 64x64 down to 4x4 which is differ from 4x4, inter CUs are also not allowed to be NxN if the CU is 8x8(4x4 compensate all). This was designed to minimize worst case memory bandwidth.

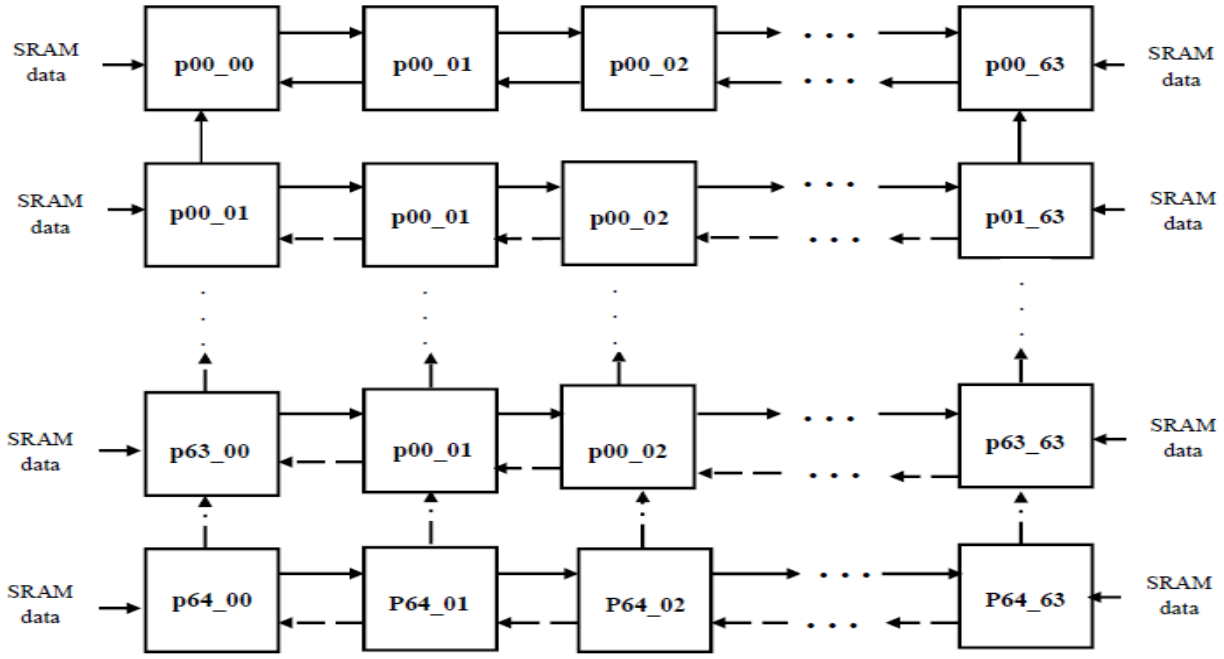

Figure-3
Search area register data flow

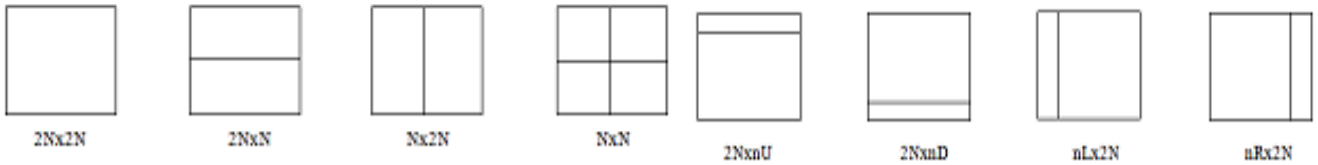

Figure-4
Different modes of splitting CB into PB

In HEVC there are 35 different intra mode, as compared to AVC there is only 9. Arrays in HEVC are twice as long as intra block size. Intra mode coding is done by building a 3-entry list of modes. These are generated along with 3-unique modes. If the mode is in the list the index will be sent otherwise sent explicitly.

SAD Summation block: The SAD values are calculated by PEs from each 4x4 values. HEVC it is designed with AMP mode and recursive quad-tree coding unit structure, so it needs 27 block sizes. The SAD summation block has the different structure by various block sizes which is different from the H.264/AVC as shown in figure 5. And the figure 5 shows the recursive quad tree coding unit structure where N=4, 8, 16 or 32. These structures are connected hierarchically and the process is similar to that of H.264/AVC. Additionally here there is a line memory which will work in AMP mode to calculate the SAD values. But our proposed method will solve the SAD value for every HEVC inter prediction mode and deeply analyze the depth of the SAD value by adding small neighbor SADs.

Motion Vector Compensation: There are two methods are used in Motion vector estimation: Signaling, Estimation. Here advanced motion vector prediction (AMVP) is used for Signaling which includes derivation of several data from reference picture and from adjacent PBs. Here merge mode is used, which allow the inheritance of MV from spatially neighboring PBs. This is designed for direct motion interference.

In HEVC MV uses a quarter-sampling precision for Estimation. In HEVC there is 7-Tap and 8-Tap filtering is used for interpolation, but in AVC there is only 6-Tap filters are used with half-sample filtering. So it can process NxM sized block which needs extra pixels in all slides to provide the filter with data. But small blocks needs more memory access which leads to more DRAM access. This leads to more cost and power due to its uni-directional transmission. HEVC supports both uni-direction and bi-direction. In transmitter there is one or two vectors are used for transmission in each PB, which will cause uni predictive or bi predictive coding.

HEVC Pipeline Process: HEVC has the tool enabled multithread decoder to decode the single prediction with tiles and wave front. In tiles pictures are divided into grid of CTBs up to 20 columns and 22 rows, each contains independently decodable CTBs. This blocks the performance and prediction unit across the tile boundaries. The single threaded decoder can simply process the tiles one by one without any rules in raster order. It can't work with each slice and slice segment. So HEVC was designed with multi-thread decoder to decode the each slice segment in the slice from the beginning to end to all the slices with common rules.

In wavefront each CTBs are decoded by its own thread. After the completion of particular thread the decoder goes to the second CTB in the row. By this method the state of the decoder is saved and transferred to the row below. By this method there is no issue of thread prediction dependency. Inter-thread communication is required to do this operation; lower thread does not suitable for higher level.

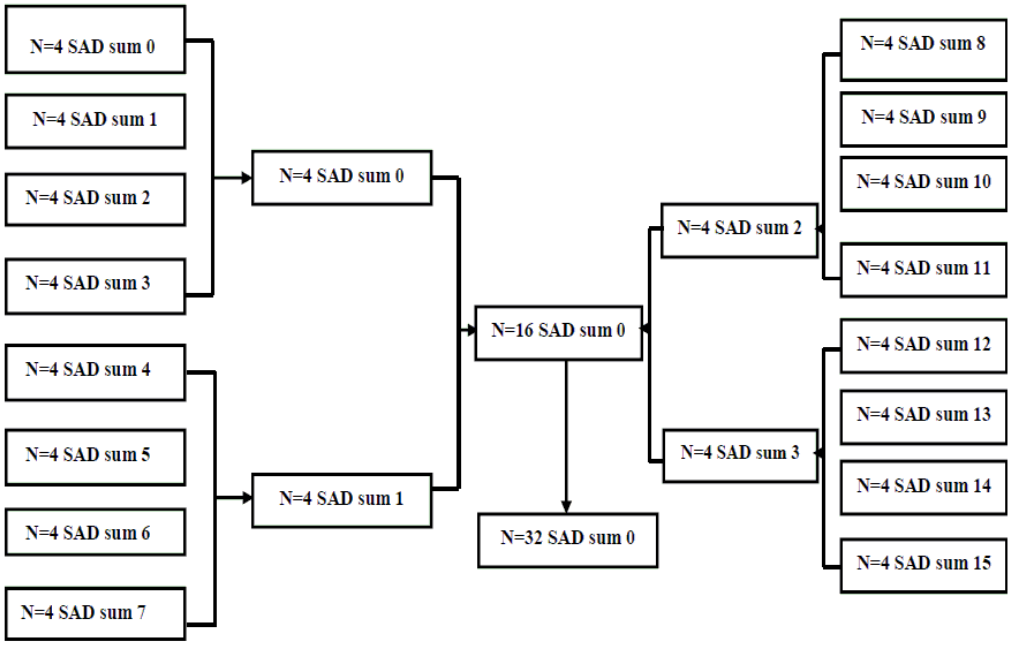

Figure-5
SAD summation block hierarchical structure

V-By-One HS

V-by-one is a high speed electrical digital signaling which will run faster than the other standard as shown in figure 6. The main use of V-by-One HS is used in data transmission. It transmits HEVC decoded bit stream for document processing and other visual media process. And V-By-One Hs is mainly designed to transmit high pixel data without timing skew problem by increasing data rate depends on the resolution requirement. V-by-One HS uses technology called SerDes and Clock recovery to achieve the high speed data upto 3.75 Gbps in each pair of cable. This will reduce the problem which affects the performance of the encoder like skew, Power consumption and Electromagnetic interface.

Equalizer and Clock Recovery: As shown in figure 6 the overall architecture for V-by-One HS is represented by individual block, which is separated by transmitter and receiver. In V-by-One HS architecture the processed bit stream output from HEVC is given to the user logic which converts the coded bit stream into data. The coded bits are given to the transmitter. The transmitter block has the Packer, Scrambler, Encoder and Serializer and the transmitted output is also mapped with training logic which receive acknowledgement from the receiver Training logic. The Serialized output from the transmitter is given to the receiver through the channels. The receiver block consist of Deserializer, Decoder and Unpacker which process reverse order from transmitter. The receiver is mapped with training logic to send the acknowledgement to transmitter. The main advantage of designing V-by-One HS is improved quality of data transmission and enables the data transmission for long distance data transfer. But there is a skew problem with the interfaces between the cables; these are avoided by the clock and data recovery. By this design V-By-One HS supports wide range of data transfer up to 3.75 Gbps by enabling low energy consumption with fixed data rate.

V-by-One HS development technology: V-by-one HS is basically designed for internal interference replacement of digital pixel displays. Here pixel data are transmitted as parallel with reduced interface while using more no of cables as well as to reduce the skew problem while using more no of cables with less space between the cables.

The architecture for HEVC with V-By-One HS transmission is shown in figure 6. The upper part of the figure represents the HEVC encoding process and the lower part represents the V-By-one HS. As shown in the figure the encoded bit stream data are transmitted through the V-By-One HS for further decoding process. Initially the encoded bit stream was given to the user logic which is the interface between the encoded data and transmitter block to convert the encoded data into bits. In the transmitter the bits from user logic are given to the packer to group the bits from user logic and the grouped bits are given to the scrambler to rearrange the order of the packer. The rearranged bits are given to the encoder to encode the bit stream encoder will be 64b/66b encoding/decoding. The encoded data is given to the Serializer to serialize the bit-stream to transmit the bit in serial. The serialized data is given to the receiver for decoding process which operates reverse order from the transmitter. The decoded output from the receiver is given to the user logic with encoded bit stream from HEVC encoder. There is one training block in the transmitter and receiver which acknowledge the received data from the receiver to transmitter to avoid the data mismatch.

The main advantage of designing V-by-One HS from other interface is equalizer and CDR technology in the Serializer and Deserializer block. By enabling the Equalizer to keep the signal integrity for more than one interface the high speed of 3.75Gbps is achieved and in addition CDR technology solves the skew problems. Due to its ability to transmit the data in the higher speed from the above description V-by-One HS is designed to reduce the no of cables, connectors and the space between the cables to reduce the skew problems with the support of wide range of transmitting speed.

HEVC video coding design with V-By-one HS transmission

The HEVC coder was designed based on the block based hybrid video coding approach. The basic source code algorithm for hybrid video coding approach is intra-picture and inter-picture prediction. Inter-picture prediction is to exploit the temporal statistical dependences and intra-picture prediction is to exploit temporal dependences. There is no any other single coding element to improve the video compression in the video coding standard. Upto decoding there is no loss of data in the compression of video coding standard. There may be a possibility of data loss in the data transmission from one medium to the other and it is avoided by the V-by-One HS transmission.

To represent the color video signal HEVC typically uses a color sampling space extension. These separate the color representation into Y, Cb and Cr component. The Y component is known as Luma and it represents the brightness. The chroma component Cb and Cr represent the color deviation from gray towards blue and red respectively. Here chroma component has the one fourth of the number of samples than the Luma in both horizontal and vertical components. Due to its property human eye has the clear vision of Luma than chroma. Each sample in the component is represented with 8b or 10b precision and 8b case is more typical than the 10b. The picture samples from the video pictures is typically sampled with rectangular sizes *WxH* as shown in the figure, where *W* represents the width and *H* represents height in the Luma samples.

As explained in the above section II the HEVC encoding has been performed. In the above process all the process are performed based on the high level syntax architecture and

operations are done by parallel process method by splitting the structure into slice.

High-Level Syntax Architecture: The design aspects of HEVC standard are to improve the flexibility for different kind of application operation and networking environments. The added features of HEVC when compare with other standard is explained as follows. In this architecture set of parameters are defined as structure, which contains the information about decoding process of several regions of decoded video which can be shared. This structure provides the robustness mechanism to the decoding process. Network Abstraction Layer (NAL) is an important parameter for high level syntax architecture, in which each syntax structure are placed into the packet data known as NAL. Here two bytes are assigned for NAL header, which is readily available to process the purpose of associated payload data.

In high level syntax architecture all the parameters are sliced into structure and each slice are decoded independently decoded from the other slices in the same picture. The main purpose of slices in the picture is resynchronization of data losses, the slice can be either entire picture or the portion of the picture. In the case of packet transmission the no of payload bits are minimized for each no of slices. Supplement Enhancement Information (SEI) syntax are used calculate the information about timing of the video pictures, interpretation, stereoscopic frame information, other display information and so on.

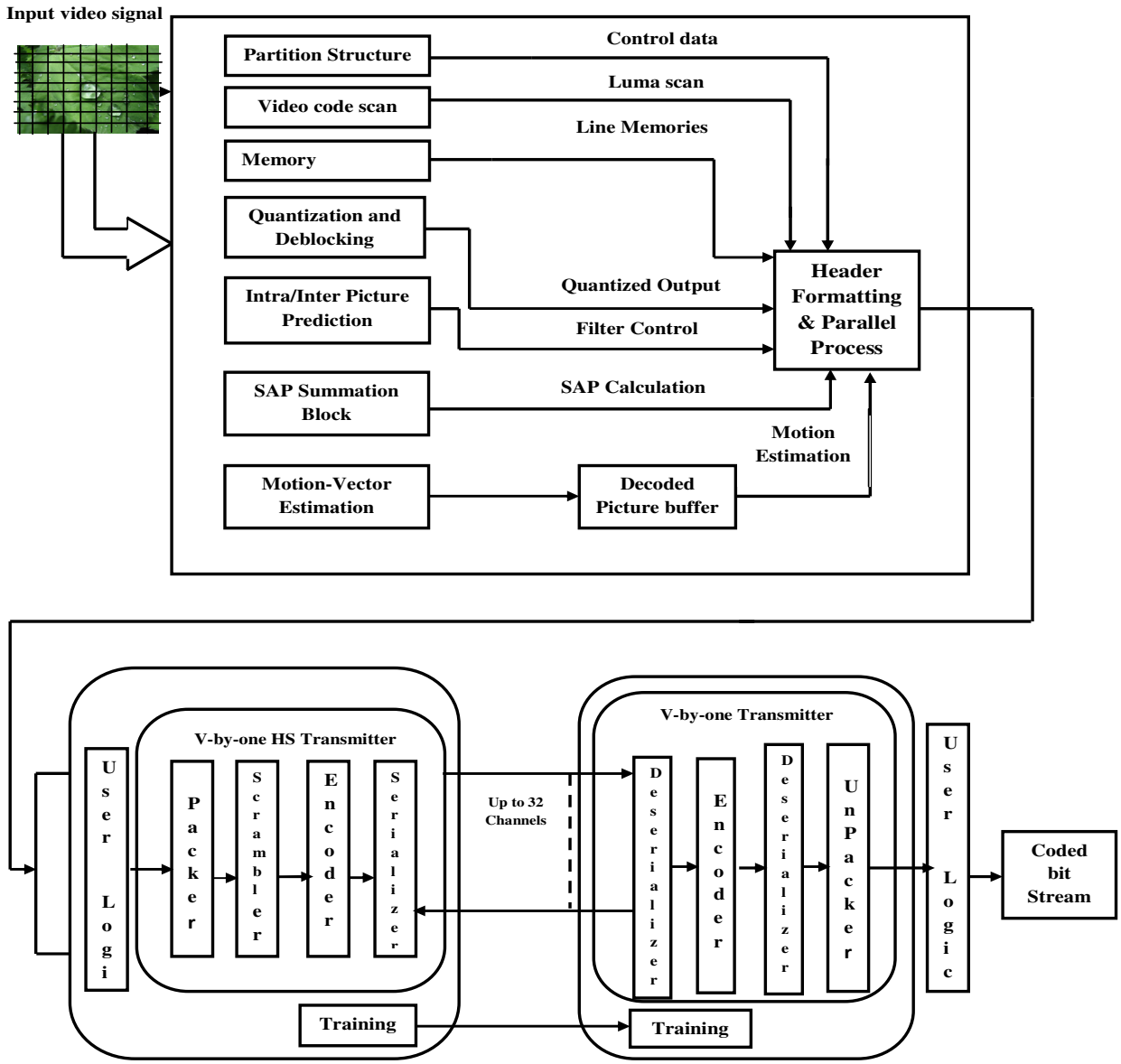

Figure-6
HEVC video encoding with V-by-One transmission

Parallel Decoding Process: The added feature in this high level architecture is parallel processing capability and structure modification of the packetization of the data. Each of the features has the individual property for the implementation of encoding and decoding. The parallel processing are performed based on tiles. Tiles are nothing but the partition of picture into rectangular region. Tiles are used to increase the speed of the parallel processing in the motion picture. Tiles are independently decoded with some data information and encoded with some byte of header information. Tiles can be additionally used in spatial random access memory to the interpicture within the video frames. A typical configuration of Tiles is performed by the segmentation of picture into rectangular frame. Tiles increase the speed of the parallelism, coarse level of granularity and avoid the sophisticated synchronization of the threads. There is a feature called Wavefront Parallel processing (WPP) used to divide the slice into the rows of CTU. The first row is processed in the ordinary way and the second rows will be processed from two CTU from the first row and so on. WPP provides the form of parallel processing rather than the granularity. The main advantage of WPP provides better compression performance than the tiles. There is a structure called dependent slice segment which is associated with the Tile to be carried out in a separate unit. This potentially makes the data to be available on the fragment packetization to be available on the packet in the single slice. The slice segment of the last part can be performed at the last part of the decoding process of slice segment has been performed. These dependent slice segments have the low-delay encoding while the others has the high in delay.

Video Code Scanning Efficiency

In HEVC scanning of video coding is performed based on Luma scanning as shown in the figure 2. In Luma scanning the performance and the limitations of the levels are calculated from the profiles, tires and levels for each picture in the frame and the limits are defined in the table 1. These three parameters are used to specify the conformance points for the implementations of various applications which has the same function.

Profiles are used to set the algorithms which are used for generation of the bit stream, where levels identify the certain parameters in the bit stream depends on the decoder process load and memory capabilities. Levels restricts the limitation of the Sample rate, Bit-rate, Picture size, Compression ratio and buffer variation that holds the compression data in decoder for data flow management and decides which one should be minimum and maximum. The levels and tires identify which bit stream is capable for decoding and conforms whether it is placed in the same tire in the same level or the lower level. From the levels and tires decoder confirms the supports of all features in the profile. But Encoder does not require any support of the feature in the profile; it requires only bit stream confirmation. Using the single level of profile we cannot achieve the required target for different applications, it is achieved by the three stages of profile Main, Main 10, Main still picture profile. From this design the no of interoperability between the devices will be reduced. These features will support for the entire device with some restriction. As described in the section II the wavelet parallel processing will be performed for singe tile only, for multiple tiles the scanning can be performed by scanning method in which each tile should have minimum of 256 samples wide and 64 samples tall. In the above three profiles the Main, Main still picture prediction will supports for only 8 bits per samples while the Main 10 supports for 10 bits per sample. The performance of motion estimation integration in HEVC standard. From the above explanation the performance of motion-vector-integration for HEVC is explained in the table 2 from gate count to operating frequency which is best in performance when compare with the previous standards. Using the AMP mode the no of memory read cycles will be reduced.

Table-1
Limitations of Levels in Luma Scanning

Levels	Max Picture Size of Luma in Samples	Max Sample rate of Luma in Samples bits per sec	Max Bit-rate of main tier (1000 bits/sec)	Max Bit-rate of High tier (1000 bits/sec)	Min compression ration
1	36 284	552 610	128	-	2
2	122 480	3 686 100	1500	-	2
2.1	245 120	7 372 200	3000	-	2
3	552 240	16 588 200	6000	-	2
3.1	982 880	33 177 150	10 000	-	2
4	2 228 104	66 846 140	12 000	30 000	4
4.1	2 228 104	133 693 410	20 000	50 000	4
5	8 912 606	267 386 220	25 000	100 000	6
5.1	8 912 606	534 773 460	40 000	160 000	8
5.2	8 912 606	1 069 547 110	60 000	240 000	8
6	35 651 084	1 069 547 110	60 000	240 000	8
6.1	35 651 084	2 139 095 000	120 000	480 000	8
6.2	35 651 084	4 278 190 008	240 000	800 000	6

Table-2
Performance of HEVC motion-estimation integration

Video Standard	HEVC
Gate count (SRAM)	3.65 M (20.23kb)
Block size	64x64 to 8x4 (27 kinds with AMP)
Search Range	64x64
Number of reference frame	1
Operating frequency	240 MHz (4K-UHD)

Conclusion

The latest HEVC technology require reduced bit rate without any loss of data in the compression. Based on the technology the HEVC has been designed with 50% reduction of bit-rate with equal quality relative to the performance[7] based on block based motion compensation of hybrid video coding standard, mainly for high resolution video, which is explained in Table 1 with no of bits and samples and the performance of the HEVC standard is explained in the table 2, which is best in the performance when compare with the previous standards. And the reason for data loss after transmitting the encoded bit stream is there is a data loss while transmitting through the transmission medium. Here using V-by-One HS this data loss can be reduced at the speed of 3.75 Gbps with constant throughput using the SerDes which is used for transmitting bits from transmitter to receiver by serially.

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