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Review Paper

An Overview of through-Silicon via – based Three Dimensional integrated Circuits (3D IC) to placement to Optimize timing

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Abstract

Semiconductor technology continues its progress in the field of 3DICs. Using stack structures through silicon via (TSV), the concept of 3D IC deals with introducing another dimension in recent designs. In fact, 3D ICs accompanying with TSV cells replace the existent connections in 2D ICs. Optimizing 3D ICs; however, is still in its early stages in many aspects. There are still some problems in locating standard and TSV cells regarding time optimization. In the present study, after queuing the layer and based on its segmentation, first we proposed a methodology for locating cells. Then, we dealt with simultaneous addressing of the pressure caused by the queuing process. Simulated fusion was applied to optimize timing and reduce wire length. Finally, an appropriate method is used to prove the procedures so that it can omit the overlaps between the cells and also the TSV cells. The results of the conducted experiments showed that both wavelength and delay in critical routes are more important in 3D ICs compared to 2D ICs.

Keywords: Through-silicon, 3D IC, optimize timing, TSV.

Introduction

Stack multilayer ICs which are usually known as 3D integrated circuits have drawn scholars' attention in recent years. The main reason for this is that 3D ICs provide more compaction density which in turn causes the performances of timing, wire length, and power to remarkably enhance. Many scholars have recently tried to develop 3D ICs. There are several major reasons for developing the technology of 3D ICs. First, one of the characteristics of 3D technology is that regarding the wire length it provides a better performance compared to 2D ICs and is considered as a substantial solution in industry after applying Moor Law. By introducing TSV, signals can connect cells possessing different layers and wire length can significantly drop. This can be gained through preventing heavy traffic in the surface. The second reason reasons for developing the technology of 3D ICs is that moving standard and TSV cells in 3D integral circuits is crucial. Although an enormous body of research has been conducted on the issue, 2D moving technology has not reached its evolution stage[1] (figure 1).

Traditional procedures of designing 2D integral circuits should be modified in order to achieve the best advantages of 3D ICs. In other words, moving algorithms in 2D ICs should be structurally examined and modified before they are used in 3D ICs. Performance-based algorithms of movement divide similar indices in order to promote the algorithms. Examine simultaneous timing of wire length. The final goal of 3D ICs is to minimize the wire length in crucial routes so that timing compression can be heightened Timing algorithms on 2D ICs can be classified into two groups named "route-based" and "network-based" algorithms. In route-based approach, delays in crucial route are directly managed. However, direct change of routes and their optimization are rather impractical because there are a lot of crucial routes. As opposed to this approach, network-based approach is simpler and also has less complexity compared to the route-based approach.

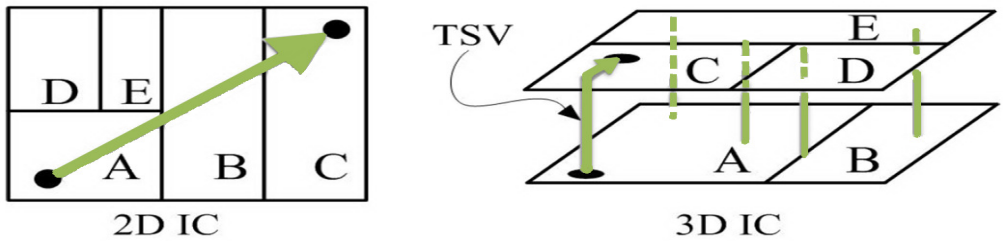

Figure-1
Internal Connections in 2D and 3D Integral Circuits

In route-based approach, timing information is converted into forms of cost amounts. Afterwards, crucial routes along with higher weights can be devoted to the crucial routes timing progress. In network-based approach, special pressures emerge and optimization is applied in order to minimize the amount of a special goal. The amount of the goal generally consists of minimizing crucial route delay or problems. However, timing should acceptably be reduced. Timing has been one of the main concerns in designing 2D integral circuits and this concern has peaked in designing 3D ICs. Standards and requirements are more important in 3D ICs compared to their similar counterparts. In this regard, timing and industrializing them require more attention. In the present study, we have proposed a timed movement based on locating design for 3D ICS.

The rest of the article is organized as follows. In section 2, we introduce movement-based classification, timing model, and problem of timed movement in 3D ICs. Section 3 presents an explanation of timed movement methodology in 3D ICs. Section 4 includes the experimental results. Afterwards, results and suggestions for further research are presented in 5 sections.

Preliminaries

Classification-based Movement: Classification-based movement is generally related to algorithm-based movement. Algorithms of classified movements are multilayer graphs that have a very high performance pace; therefore, they are more appropriate in large scales. Timing problem can be considered in locating the wire by adding extra timing cost in the classified algorithm[1]. By searching the cut lines, classification-based movement is involved with dividing Mira environment into independent sections. Similarly, the overall design is divided into a lot of sub-circuits. Every sub-circuit, in turn, is assigned to an independent section. This process repeats as many times as the amount of the goal or the number of the cuts minimize. In our performance stage, we finish the process so that the size of the sub-circuits reduces as the smallest section as possible. In designing standard cells, classification continues as far as the size of locating area becomes equal to the row height and during verification stage the cells can locate in the rows[2].

Generally, movement-based classification is based on Fiduccia Mattheyses' classification algorithm. This mechanism is based on cell gains. First, primary cell gains are evaluated then cell movement is discussed, which have the greatest gain. After movement of the cells with high gains, updating the list of gains continues as far as the cells move. After the total gains have been assessed, this process finishes. Finally, the utmost total gains are removed and cells that are connected to specials areas are moved. The utmost gain means that there will be the least cut between two groups of separated cells. Process of alternative movement will end when cells with negative gains move, too[3].

Classification-based movement means that the total number of cuts between two sub-circuits and balance areas reduces simultaneously in both areas. Through the conducted experiments, we concluded that groups have connected cells which have a cluster form and cause the performance time to increase and the size of the cut between two sub-circuits to optimize[4].

Timing Model: In order to analyze the timing process, Elmore's delay model is applied so as to assess connected delay and delay in TSV cells. Implementing TSV and connected delay model is derived from [5] (figure 2).

Delay (T) from the beginning to the end can be modeled as follows (1).

$$T = R_d(C_w + C_l) + C_l R_w + \frac{1}{2} C_w R_w \quad (1)$$

Where: R_w is wire resistance, C_w is the existent capacity, R_d is the driving output resistance, and C_l is loading capacity of the receivers. This formulation can be replaced by another equation.

$$T = \frac{1}{2} rcL^2 + (cR_d + rC_l)L + \frac{1}{2} R_d C_l \quad (2)$$

Where: r is the resistance unit of wire length and c is the capacity unit of wire length.

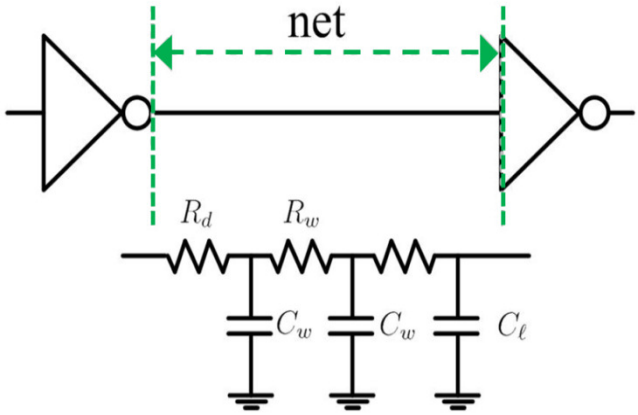

Figure-2
Elmore's Delay Model

Designing delay models of TSV is an important aspect in analyzing 3D static timing. Due to having the extra dimension of z, a new delay model can be achieved to assess the timing of z dimension. Here, inducing effect is taken into consideration and the analysis of z dimension timing can be implemented into Elmore's delay model. The delay of TSV cell is one of the connected delays. Noisiness of TSV cell is explained in Mohammad Aghaei et al[6] and Cong J. et al[7]. Resistance of TSV cell (R_{TSV}) is a function of conductivity and cross-sectional environment, capacity of a single TSV cell (C_{TSV}) and Elmore's delay form for TSV cells, which is explained as follows (figure 3).

$$T_{TSV} = \frac{1}{2}rcL^2 + (cR_{TSV} + rC_{TSV})L + R_{TSV}C_{TSV} \quad (3)$$

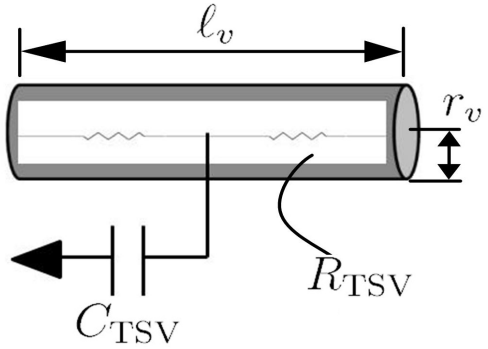

Figure-3
TSV Delay Model

$$R_{TSV} = \frac{l_v}{\sigma\pi r_v^2} \quad (4)$$

$$C_{TSV} = \frac{63.34\epsilon_0 l_v}{\ln(1+5.26\frac{l_v}{r_v})} \quad (5)$$

Where: l_v is TSV length (um), r_v is TSV radius (um), σ is sub-layer conductivity, and ε_0 is electricity unit of measurement.

Formulation of the Problem: Timing problem in 3D ICs can be explained as follows. Considering the graph of G(C, E) which is equal to file definition (def); C and E stand for the cell and the edge, respectively. The number of the moving cells is n. Each cell is $c \in C = \{c_1, c_2, ..., c_n\}$ and its coordinate can be defined as (x_i, y_i, z_i). After 3D layers are assigned to them, the cells will distribute on their special layers[8,9]. A guided edge like $e = (a,b) \in E = \{e_1, e_2, ..., e_n\}$ means that signal direction, constituting cell form of $a \in C$ is $b \in C$. Primary input/output pads cause limitations for the underlying layer that has coordinates with constant characteristics. A number of 3D ICs through m are located in different layers. Each 3D IC makes a connection through $v \in TSV = \{v_1, v_2, ..., v_m\}$. Integral circuit timing introduces two metric units: WNS and TNS. WNS is the worst slack in all final points of timing. Timed points also show the input and output sections of a cell or the first input/output pads of the circuit. TNS is the timed final points which have a negative crack. For every timed point (i), the input time is ($T_{arrival}$). The signal reaches the timed points and the require time means the time that the signal requires at the timed point. The timed crack means that the signals enter and then go into a stage where they need time. All mentioned above can be summarized as follows[10]:

$$T_{arrival}(i) = \max_{\forall j \in fanin(i)} \{T_{arrival}(i) + T_{inst}(i) + delay(j,i)\} \quad (6)$$

$$T_{arrival}(i) = \min_{\forall j \in fanin(i)} \{T_{required}(j) - T_{inst}(j) - delay(i,j)\} \quad (7)$$

Calculation model of wire length in a network is like a closed box in which all network connections can be seen and this can be achieved by calculating half of the perimeter of the primary wire length[11].

$$HPWL(e) = \left(\max_{ct \in e}\{xi\} - \max_{ct \in e}\{xi\}\right) + \left(\max_{ct \in e}\{yi\} - \max_{ct \in e}\{yi\}\right) \quad (8)$$

$$TSV(e) = \left(\max_{ct \in e}\{zi\} - \min_{ct \in e}\{zi\}\right) \quad (9)$$

Where: e is the network, ci is the cell, and all coordinates are (x_i, y_i, z_i).

Our main purpose is to find a systematic locating in TSV cells without any overlaps. At the same time, 3D IC designs can help achieve a better timing performance and reduce wire length, the number of TNS and WNS, and delay on the crucial routes. All over this process, TSV cells continually face balance barriers[12,13].

Timed Locating Methodology in 3D ICs: Our Methodology Flow: In this section, timed locating algorithm for 3Dclassification which has both sections of time and TSV is presented. The applied methodology is presented in figure 4. This section is organized as follows. First explains classification-based locating and allocation of TSV cellcoordinates[14]. Next, Elmore's delay model and analysis of connected delays in TSV cells are presented. In next section, describes timing optimization through Elmore's delay model and analysis of internal connections and explains systematization process of locating methods. Finally, the method of pressure allocation in TSV locating is explained[15,16].

Classification-based Locating in 3D ICs: The procedure begins with classifying the 2D circuit and converting it into a 3D design. 3D locating area is achieved by dividing the 2D classification area into some layers, which is presented in Figure 5. The width of the cell reduces through multiplying it into the ratio of $\frac{1}{\sqrt{nl}}$, where: *nl* is the number of the layers. The area of the cell reduces to $\frac{1}{nl}$ and the total movement area is equal to 2D scale[17,18].

Connected mechanism in 3D ICs is achieved through TSV cells and that is why movement of TSV cells affects the total length of the wire and timing performance. The number of TSV cells that require signals in all their layers is specified after each layer has been allocated to a cell. In this stage, TSV cells can cause wire length to decrease. The whole area that occupies the TSV cell is almost wide. Therefore, the overall area and sing TSV cells should be taken into consideration[19].

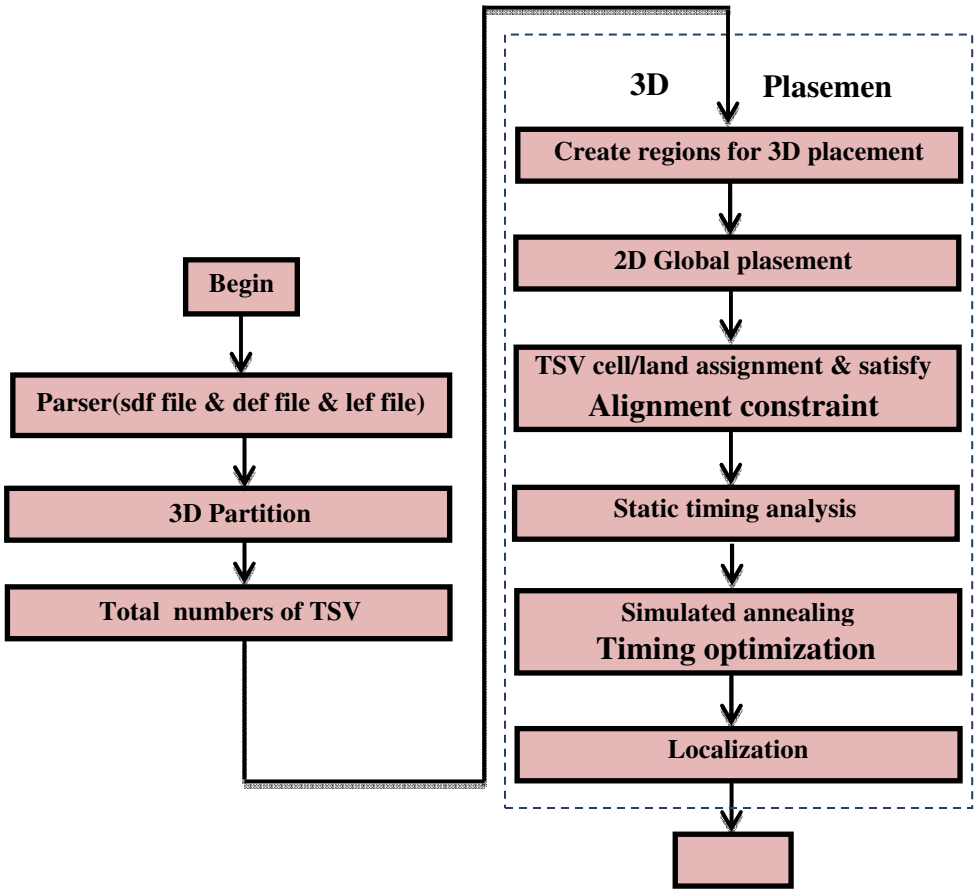

Figure-4
Methodology Flow

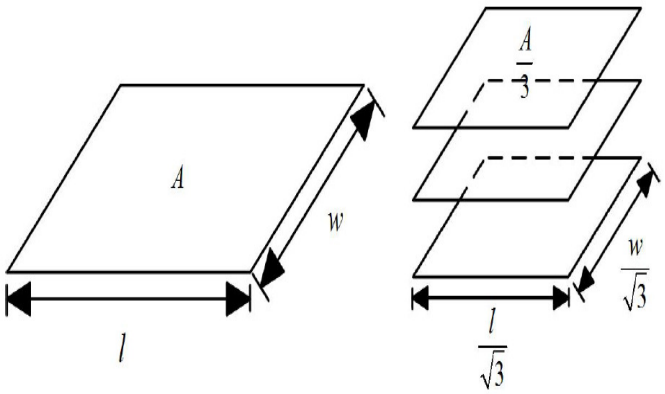

Figure-5
Patterns of 2D and 3D Movements (A stands for area)

In order to prevent an increase in TSV cells and keep the overall logical length of the wire in 2D plane, the problem of 3D ICs was simplified through classification-based replacement. Regular and unreasonable performance of the layers from top to the bottom helps standardize the cells through vertical cuts. Each plane can use a two-section method in its row status. In each cycle, cells will be allocated to a specific layer. The process of general locating completes after the alternative classification ends[20, 21].

The difference between 2D and 3D ICs is that 3D circuits can transmit signals through TSV. In other words, cells in different layers connect to each other through TSV. Different locating of TSV cells leads to different delays. If TSV cells are too far from typical cells, more communication delays may be observed. As opposed to this, if TSV cells are located near special cells where the signals can transmit without any delay, a more favorable condition will be expected[22].

Coordinate of the cells is specified after classification-based locating. Afterwards, coordinate of the TSV cells can be determined. First, the ratio of average number of TSV cells to the rows is specified. There are a lot of advantages in this method. One of these advantages is that the row has an average distribution for its TSV cells so that it cannot create a huge density for TSV cells. Another advantage is that TSV cells have more opportunities to exchange between different rows[23, 24].

Coordinate of TSV cells is specified through calculating the center of the box containing the circuits; therefore, TSV cell coordinate is related to the cell coordinate. The main reason for

this is shorter wire length and the minimum cost. The box center (x, y) is assigned through the smallest and the largest coordinate of x cells and calculation of y coordinate is carried out in the same way. This stage is a set of primary coordinates for TSV cells[25] (figure 6).

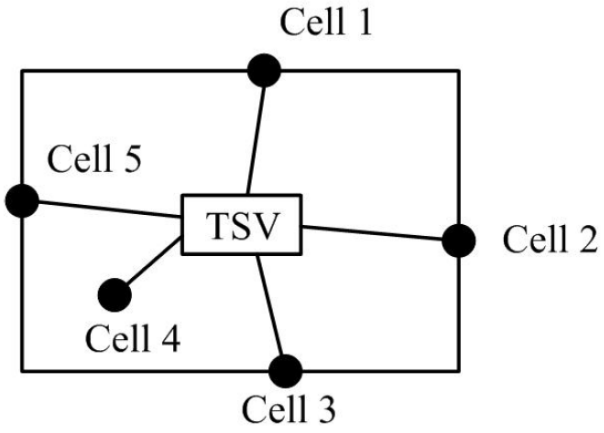

Figure-6
Primary Allocation of TSV

After the initial configurations, the cells are separately placed in a row[26]. This is the method of configuration for TSV distribution row (the row which has distribution of the TSV cells). When the coordinates of TSV cells are specified and allocated, the connection between the signals in different layers can be corrected. The delay time of the circuit can be specified through a timed model, cells completion, and connections of TSV cells[27].

TSV cells placement
for layer=top to bottom do
for TSV-distribution row do
1. get TSV distribution
2. initial TSV cells assignment
center of bounding box calculation
3. find a best row
4. set TSV cells to appropriate coordinates
5. link signal
end
end

Set TSV cells to appropriate coordinates
for TSV-distribution row r do
if(r has free TSV cells)
1. cost calculation for r $cost_r$
$cost_r$ = coordinates y of r - initial y of TSV cell
2. choose the smallest cost $cost_r$ (the nearest row)
3. set y coordinates of TSV cell
end

Queuing Area: Existent signals in different layers are verified by the TSV cell. When a TSV cell is specified, redistribution cost of the layer (RDL) can decrease. To guarantee satisfaction from the method, TSV cells in the layer of i (the top layer) should be placed along with landing cells in the layer of i-1 (the layer located lower than distribution of TSV cells). Following this method, more accurate connections can be created between small and landing pads[28] (figure 7).

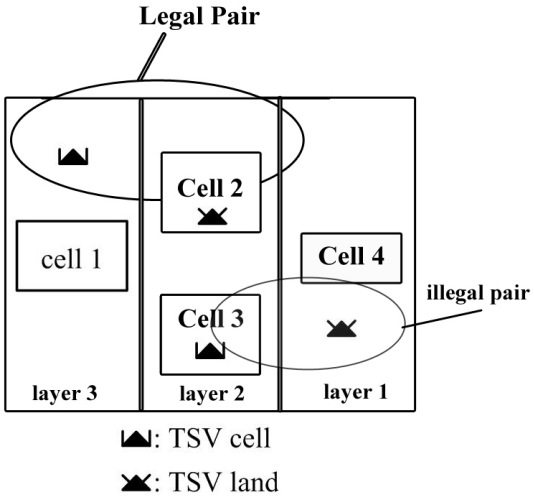

Figure-7
TSV Queuing Area

The coordinate of TSV cells should be specified for delay calculations. In order to prevent the problem of overlap between cells with TSV cells, movement is carried out in another way. A method is introduced into resolve the problem[29]. This method provides movement flow from the top layers to the bottom ones which can always do queuing area correctly. TSV cells in every layer will have no overlaps with any other cells[30]. As opposed to this, if TSV cells are specified, they will be observed from bottom layers to top layers because no TSV cell is available in the bottom layer and only landing cells will be specified. TSV cells in the top layer are applied to provide the row area and they can cause some problems to TSV cells and overlaps between cells in similar layers[31].

In order to collect these values, queuing area should be considered in 3D ICs. The main idea is also applied in this procedure. TSV cells are specified from the top layer to the bottom one so that no overlap between TSV cells and gained cells in the experimental results can be observed.

Simulated Fusion-based Timed Movement: Simulated fusion is applied for progress and optimization of the timing in our timing movement. Simulate fusion algorithm is a kind of fusion process which is achieved through appropriate justification of cost functions in order to achieve appropriate performance. The cost of an inter-cell exchange is specified based on the connection edge. Decision for a cell exchange is made based on the exchange costs. If the total costs are positive, the cell starts

exchanging successfully. But if they are negative, it fails to exchange[32].

Allocated cells have small cracks which manage the most critical conditions. This criticality is described as follows:

$$\text{Criticality(i, j)} = 1 - \frac{\text{Slack(i,j)}}{\text{Criticality Path Delay}} \quad (10)$$

Here

$$Slack(i,j) = T_{required}(j) - T_{arrival}(i) - delay(i,j), T_{required}(j).$$

Where: $T_{arrival}(i)$ is the require time of cell j, $T_{arrival}(i)$ is the time of entering to cell i, and the delay (i, j) is a connection delay between cells i and j.

Here we introduce the cost function in performing movement timing. The cost function only considers the wire length and the network timing. Wire length performance and timing optimization are our main purposes. We try to achieve a better timing performance without an increase in wire length. In this regard, we use sections of wire-cost (11) and time-cost (13) as our cost function[32].

$$\text{Wire} - \text{Cost} = \sum_{e=1}^{\text{Nets}} [\text{HPWL(e)} + \text{TSV(e)}] \quad (11)$$

$$\text{Time} - \text{Cost(i, j)} = \text{delay(i, j)}.\text{Criticality(i, j)}^{\text{Criticality}-\text{Exponent}} \quad (12)$$

$$\text{Time} - \text{Cost} = \sum_{\forall i,j \in \text{cell}} \text{Time} - \text{Cost(i, j)} \quad (13)$$

$$\Delta C = \lambda . \frac{\Delta \text{Time} - \text{Cost}}{\text{Previous Time} - \text{Cost}}$$

$$+(1-\lambda).=. \frac{\Delta \text{Wire}-\text{Cost}}{\text{PreviousWire}-\text{Cost}} \quad (14)$$

Generalization: After total locating, there will still be overlaps between standard cells and TSV cells. We apply a special algorithm on the generalized algorithm of Tetris. Our method is similar to Tetris method along with a few modifications where the modifications make it possible for it to be used in 3D ICs. TSV cells are first generalized then standard cells will be.

Generalizing TSV: There may be some overlaps between TSV cells in a row. In average cell distribution for a row, only modification and calculation x coordinate are taken into account. Coordinate of y in TSV cell was specified during the primary movement. Only distributed TSV cells in a row are considered in distribution. First, all TSV cells in a row are considered and new coordinate of x is calculated in X_c which is in fact located in the box center. The reason for this is that the coordinates of the cells may change after locating in order to enhance the performance; therefore, this box is not in a similar network with a primary allocation status. Second, their classification is based on their x coordinates. If the TSV cell still continues overlapping other TSV cells after re-modifying its coordinate, its precise calculation of x coordinate will be carried out. The exact coordinate of x in $X_i$is calculated after computing its costs[33]. An appropriate coordinate should include the minimum cost. Its method is as follows:

TSV legalization
for each row r do
1. r → getTSVCell
2. calculate center X_c of bounding-box
3. sort them according to X_c
4. if(still overlap with another TSV cells)
   calculate legal coordinates X_ℓ
   calculate cost_diff = abs(X_ℓ, X_c)
5. choose minimum cost_diff
6. set legal coordinates X_ℓ for TSV cell
end

Cell Generalization: After generalizing the TSV cell, we cope with the existent barrier on the way of these cells. The only thing that is required is management of the overlaps between the cells. Similar generalization has Tetris status. If the row width is not enough, the nearest row with similar direction will be found and then adjusted[34].

Cell legalization
for each row r do
1. r → getTSV
2. calculate useful region for cells
3. if(cell overlap with another cell in the useful region)
   replace cell on this row
   if(over row width)
   choose the nearest row which has
   the same direction with the cell
   end if
end for

Experimental Results

This algorithm has been compiled using C++. A computer with adual-coreprocessor,3GHzcache,and4096MB of RA Min Linux has been used. In the present study, our basic criteria are ISCAS85downloaded from[35].

The circuit has been explained in LEF/DEF format and the internal delays create standard delay files in sdf format. We modify 2D integral circuits in designing 3D ICs. This area reduces into $\frac{1}{nl}$ where nl stands for the number of the layers. The pad situation has changed a little. After classifying the circuit, we create a locating circuit that has the largest area in these three layers. The area of the layer contains TSV cells. All of the inputs and outputs are located in the lower layer. The area of the TSV IO is 85 square micrometers. This figure is 255 square micrometers for the TSV cell. The ration of standard side cell in this area is 1.13:1. Table 1 presents the basic standard characteristics. Table 4 also presents the results of three-layer locating[36,37].

Figure 4 shows the related technology along with the locating results c1908, TSV cells and their distribution, a red line which means the locating area, average blue blocks that mean TSV sections, green blocks which show TSV cells, and blue blocks that present the cells. TSV status on the layer of i-1 is allocated to TSV cell on the layer of i.

Table-1
Basic Standard Characteristics ISCAS85 after Classifying the 3D IC

Input File	TSV Cell Number	TSV Section Number	Cell Number
c1908	105	105	880
c2670	403	403	1269
c3540	139	139	1669
c5315	330	330	2307
c7552	531	531	3513

Table-2
2D Movement after Generalization

Circuit	HPWL	Critical Route	TNS	WNS (ps)
c1908	73552.27	46970.87	28	-0.002
c2670	132360.72	38142.38	28	-0.002
c3540	197642.19	55242.35	28	-0.002
c5315	249188.64	57428.66	28	-0.004
c7552	480862.28	50797.82	28	-0.004

Table-3
3D Locating after Generalization and Specifying the Area

Circuit	HPWL	Critical Route	TNS	WNS (ps)
c1908	39964.83	46923.97	28	-0.006
c2670	97814.48	38083.8	0	0
c3540	110990.16	54902.31	0	0
c5315	181797.53	57177.56	28	-0.004
c7552	286605.88	50379.83	28	0.002

Table-4
Locating after Generalization and Specifying the Area

Circuit	HPWL	Critical Route	TNS	WNS (ps)
c1908	32086.79	46891.95	28	-0.004
c2670	72576.26	37821.84	14	-0.001
c3540	78743.85	54861.85	0	0
c5315	161172.89	57208.76	7	-0.0007
	205572.98	50315.58	228	-0.002

Conclusion

In the present study, we have presented an alternative 3D procedure containing timing analysis. TSV cells were created through algorithms of classification-based locating. Allocating TSV cells always pushes aside adaptation barriers[37]. Is shown at figure 8 and table 5.

Table-5
3D ICs Locating Progress Compared to 2D ICs

Circuit	Layer Number	HPWL	Critical Route (PS)
c1908	3	44.66%	0.1%
c1908	4	53.38%	0.16%
c2670	3	24.1%	0.14%
c2670	4	46.17%	0.87%
c3540	3	41.81%	0.63%
c3540	4	59.13%	0.66%
c5315	3	26.12%	0.47%
c5315	4	33.32%	0.34%
c7552	3	39.9%	0.81%
c7552	4	56.24%	0.94%

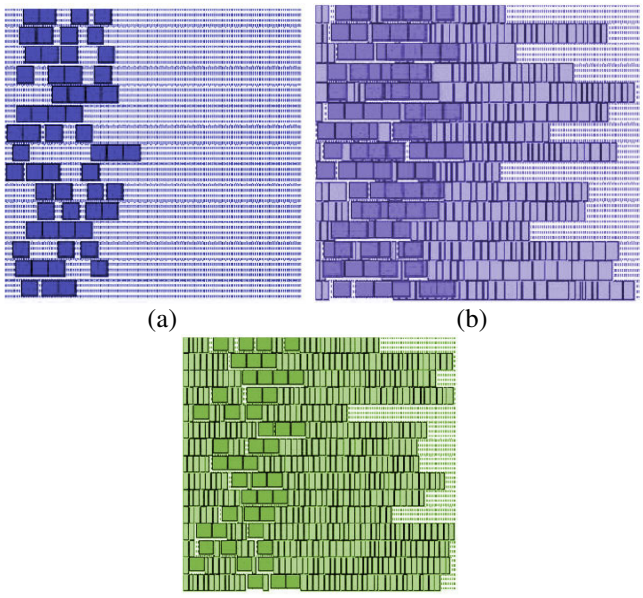

Figure-8
TSV based Movement in Three-layer Section: (a) The Lower Layer, (b) The Middle Layer, (c) The Top Layer

In this paper, a thermal control mechanism with an in-situ temperature sensor for TSV 3D-ICs is presented using thermal guard rings and thermal TSVs. Depending on the thermal guard ring and thermal TSVs, an analytical model for on-chip heat dissipation in each power-thermal domain is also presented in this paper. Based on the analytical model, the offset temperatures between the hotspots in the power-thermal domain and thermal guard ring can be calculated. Therefore, the in-situ temperature sensor is placed near the thermal guard ring to detect the temperature and feedback the thermal information for the system. The simulation results show the thermal control mechanism with an in-situ temperature sensor can reduce temperature and detect heat dissipation of TSV 3D-Ics significantly. The proposed thermal control mechanism can further achieve about 25.10% temperature reduction. This technique can be extended to balance workloads in the overall system for further reducing temperature. In the future, the most

important issue is that the models should be able to carry out timing analyses better. This is necessary for calculating the delays. The correct model of TSV cell in physical design of 3D ICs is vital.

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