Research Journal of Recent Sciences _____ ISSN 2277-2502
Vol. **2(6),** 23-31, June **(2013)** *Res.J.Recent Sci.*

Analysis and Design of a Novel Junctionless Triple Metal Cylindrical Surround Gate (JLTM CSG) MOSFET

Gupta Santosh Kumar[1], Baishya Srimanta[2]
[1]Department of Electronics and Communication Engineering, Motilal Nehru National Institute of Technology Allahabad, UP– 211004, INDIA
[2]Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam – 788010, INDIA

Available online at: www.isca.in
Received 28th January 2013, revised 12th February 2013, accepted 12th March 2013

Abstract

All transistors in use currently are based upon the laws of junctions. But due to dimensional scaling of the MOS transistors, the fabrication of the lower dimensional MOSFETs is becoming difficult due to the presence of the two junctions at source and drain sides. There is also decrement in the ON state current due to smaller dimensions of the transistors, since the current mainly flows through the inversion layer created at the SiO_2/Si interface. One alternate option for the improvement of the above mentioned characteristics was demonstrated by Colinge et. al. by Junctionless (JL) Transistors in the year 2010, which was conceptualized and patented by Lilienfield in 1925. The effect of the dimensional scaling on JL transistors are still to be explored in submicron regime. Being the depletion mode device, the JL devices are normally ON even in the absentia of the gate potential. So, to turn these devices OFF, one has to apply a gate potential. In this paper we propose a JL cylindrical surrounding gate (CSG) MOSFET using triple metal gate (TMG) structure to overcome this limitation of the Junctionless transistors. With the use of the TMG structure, many other parameters have also been observed to be improved. The analog and RF parameters of proposed junction less triple metal cylindrical surrounding gate (JLTM CSG) MOSFETs like transconductance, transconductance generation factor, intrinsic gain, early voltage, cutoff frequency, maximum frequency of oscillation, gain bandwidth product etc. have been verified to be also improved using the extensive 3D TCAD simulations.

Keywords: Junctionless, triple metal gate, cylindrical surrounding gate, analog, RF, TCAD

Introduction

Due to the aggressive scaling of transistor the sizes are now of nanoscale regime. At these sizes it is very hard to control the sharp source/drain-channel junctions' from the device fabrication point of view. However, if the junctions are removed by forming the source/drain and gate of same type of material then also it is possible to get a transistor like action called as Junction Less (JL) transistors. The idea was first filed for patent by Julius Edgar Lilienfield on 22nd October 1925[1,2] . This device was recently fabricated by Colinge et. al[3] at Tyndall National Institute with gate length of $1\mu m$. These transistors are quite different than the conventional junction transistors in terms of working. Since there is no junction involved hence the device sizes can be scaled to very low dimensions. This will decrease the transit time of the carriers across the channel leading to high performance transistors. The device is turned OFF by applying a proper gate biasing voltage to deplete the channel charges; hence the channel thickness has to be taken at most to the maximum depletion depth that can be obtained, typically 10 nm or less[3-9].

Haijun et al[9] and Santosh et al[10] has recently reported a Junctionless MOSFET using dual metal gate structure using 3D numerical simulations. They have reported excellent properties of the dual metal structure at lower gate voltage overdrive. The gate length ratio and workfunction difference significantly affect the transistor characteristics.

At extremely short gate lengths of 100 nm and below the short channel effects (SCEs) can be seen to be dominating as is observed in the conventional (with junction) or inversion mode transistors. For minimizing this effect a surround gate structure with cylindrical cross section looks to be promising, because it controls the channel from all around. To further reduce the SCEs, similar to inversion mode transistors, the gate material engineering using triple metal gate structure has been proposed in this paper below 100 nm gate length. A 3D TCAD simulation has been carried out to evaluate the analog and RF performance of the proposed junction less triple metal cylindrical surround gate (JLTM CSG) MOSFETs.

The paper is arranged in following IV sections. In section II the generic JLTM MOSFET structure parameters has been explained. In the section III, first the DC characteristics of JLTM MOSFETs have been extracted and compared with a junction less single metal (JLSM) MOSFET of identical dimensions. In the latter part of the section, the analog parameters of JLTM have been compared with JLSM. Section IV shows the scaling of different DC, analog and RF performance parameters with gate length scaling of the JLTM MOSFETs.

Methodology

Device Fabrication

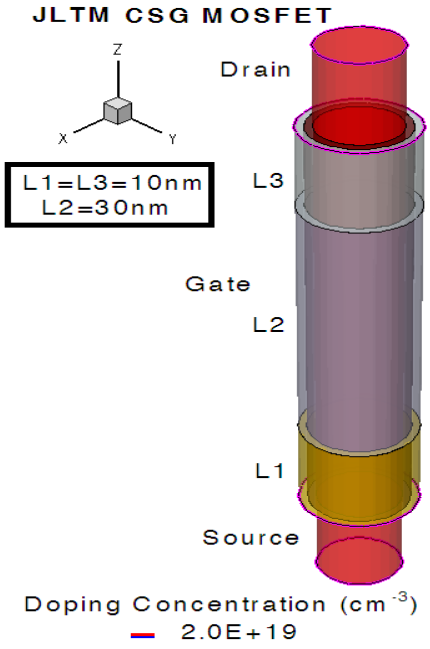

Figure-1
3D view of Junctionless Triple Metal Cylindrical Surrounding Gate (JLTM CSG) MOSFET

JLTM CSG MOSFET's structure as shown in figure-1, were generated using the sentaurus structure editor tool of the synopsys sentaurus TCAD. A typical device structure with triple gate structure is shown as in figure-1 with $L1 = L3 = 10nm$, $L2 = 30nm$ and $R = 10nm$. Highly doped silicon with $2.0\times10^{+19}cm^{-3}$ (arsenic) was used as source/drain and channel regions. The three laterally contacting gate materials used are Gold (workfunction, $\phi_{M1} = 4.8eV$), tungsten $\phi_{M2} = 4.6eV$ and titanium ($\phi_{M3} = 4.4eV$) respectively. The gate oxide thickness (SiO_2) has been taken to be $1nm$ for all the devices under consideration. The results of JLTM has been compared with a typical junction less single metal (JLSM) CSG MOSFET of gate length $30nm$ (titanium) with all other device parameters taken to be identical.

The device has been simulated using 3D device simulation tool sentaurus device of synopsys sentaurus TCAD. Poisson's equations with density gradient models have been solved for the JLTM and JLSM CSG MOSFETs both. Density gradient quantization models applicable for the simulations of quantum wells, SOI structures and MOSFETs have been used to get reasonable description of terminal characteristics. These devices are first simulated to get the DC and analog characteristics and later ac simulations have been carried out to extract the RF characteristics.

Results and Discussion

Electrical characteristics: Figure-2(a), 2(b), 2(c) and 2(d) compare the electrostatic potential, electron density, electric field and electron velocity respectively at the SiO_2/Si interface. Electrostatic potential under the gate $M1$ of JLTM CSG $(L1)$ does not change with changes in V_{DS} due to the use of triple metal structure in the gate. This effectively reduces the SCEs. Electron density at the source end is higher for the JLTM CSG. Electric field for the JLTM CSG is higher at the source/drain ends. The higher electric field at the source end is good in the sense it provides higher injection velocity of the carriers into the channel from the source, but, the higher electric field at the drain end may lead to hot carrier effects (HCEs). Electron velocity is relatively lower for the JLTM CSG because of the lower electric field in the direction of the current flow along the channel.

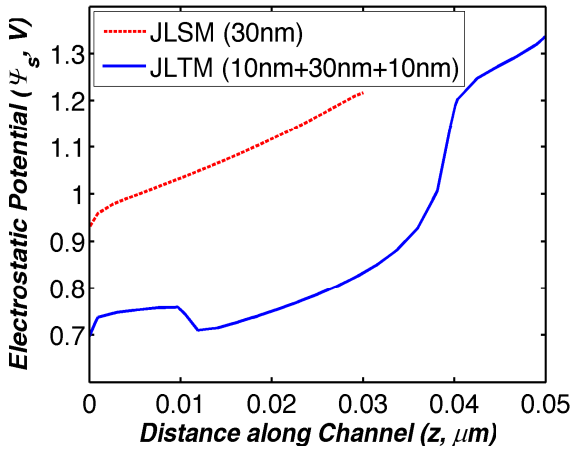

Figure-2(a)
Surface Electrostatic potential (Ψ_s) at $V_{GS} = V_{DS} = 1.0V$

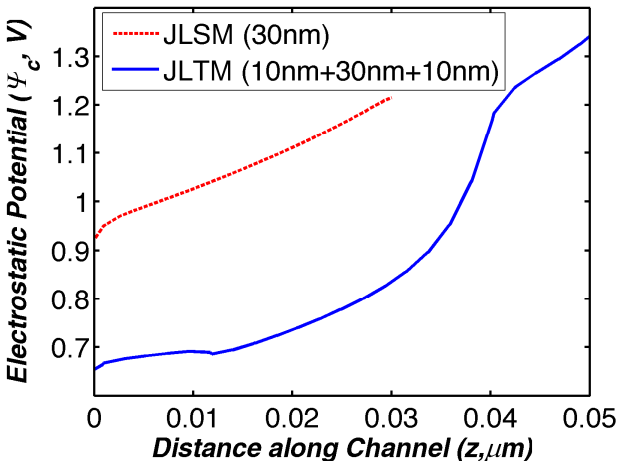

Figure-2(b)
Electrostatic potential in the center of (Ψ_c) at $V_{GS} = V_{DS} = 1.0V$

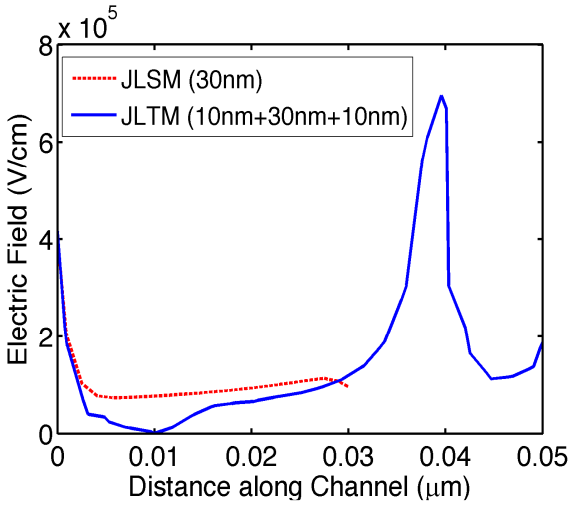

Figure-2(c)

Electric field at $V_{GS} = V_{DS} = 1.0V$

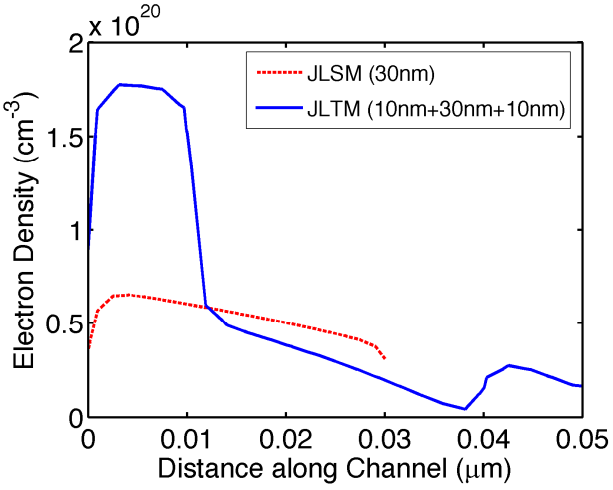

Figure-2(d)

Electron density at $V_{GS} = V_{DS} = 1.0V$

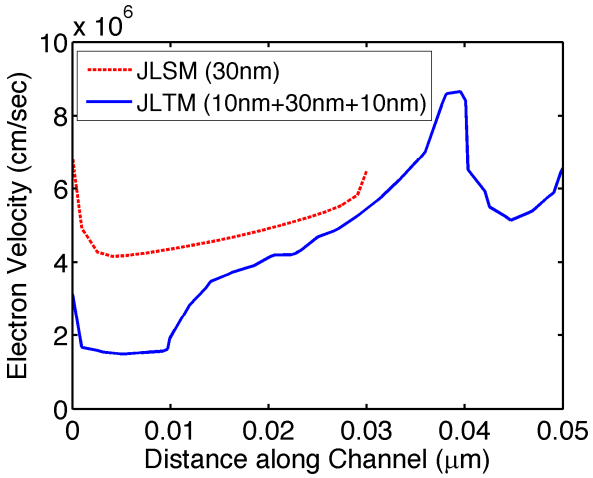

Figure-2(e)

Electron velocity at $V_{GS} = V_{DS} = 1.0V$

DC Characteristics: The ON and OFF state currents are shown in Figure-3(a) and 3(b) respectively. As can be observed that the ON state current for the **JLTM CSG** is larger by more than 1.5 times as compared to the **JLSM CSG** and at the same time the OFF state current is also smaller 10^4 times. Reduction in OFF state current results due to the triple metal gate structure used which screens the drain voltage variations. For digital applications the I_{ON}/I_{OFF} ratio is very important. This ratio is very high for the JLTM MOSFETs as compared to JLSM.

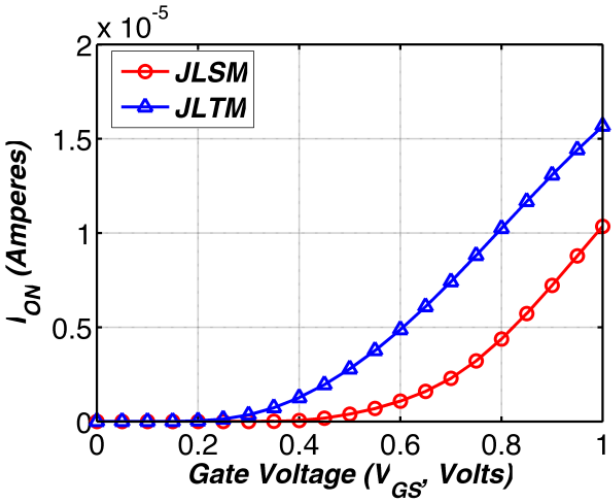

Figure-3(a)

ON state current $(V_{DS} = 1.0V)$

Analog Characteristics: The different analog performance parameters of interest are the output resistance (R_0), conductance (ϑ_d), trans-conductance (ϑ_d), trans-conductance generation factor $(TGF, g_m/I_D)$, intrinsic gain $(g_m R_o \text{ or } g_m/g_d)$ and early voltage (V_{EA}).

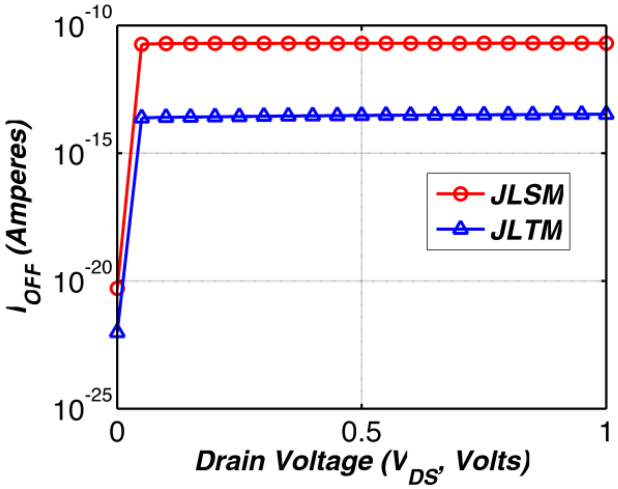

Figure-3(b)

OFF state current $(V_{GS} = 0.0V)$

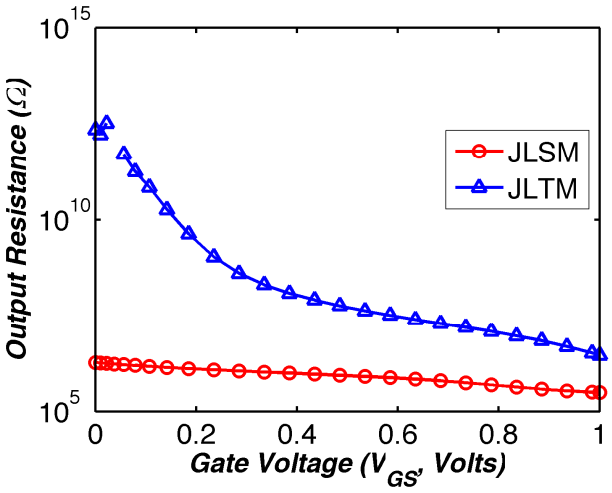

Figure-4(a)

Output resistance (R_o) **at** $(V_{DS} = 1.0V)$

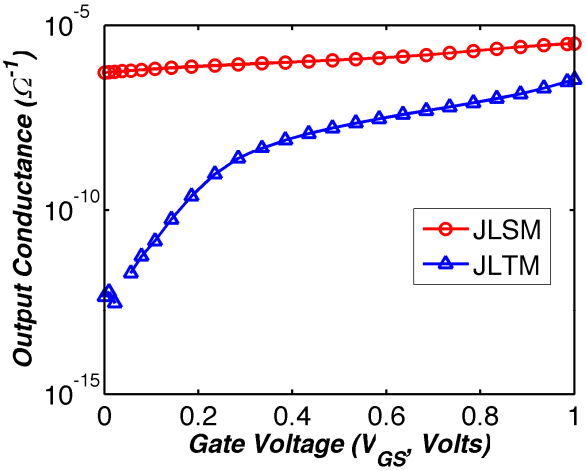

Figure-4(b)

Output conductance (g_d) **at** $(V_{DS} = 1.0V)$

Figure-4(a) and 4(b) compares the output resistance and conductance respectively of JLTM and JLSM. Output resistance of JLTM is larger and hence conductance is lower than the JLSM due to increased channel length of the former. This is also one of the reasons responsible for the reduced ON state current. Transconductance (figure-5(a)) of JLSM is higher at lower operating voltage $(upto \sim 0.5V)$ but once the JLTM is turned ON $(\sim 0.8V)$, it provides significantly higher values. The intrinsic gain (figure-5(b)) of the JLTM is significantly higher (approximately 2 times in dB) as compared to the JLSM counterpart. The TGF is considered as available gain per unit power dissipation. TGF of JLTM, figure-5(c) is more than 8 times larger to that of JLSM which shows that for getting a desired gain less power will be required by the former device. It makes JLTM a strong candidate for low power analog applications as well.

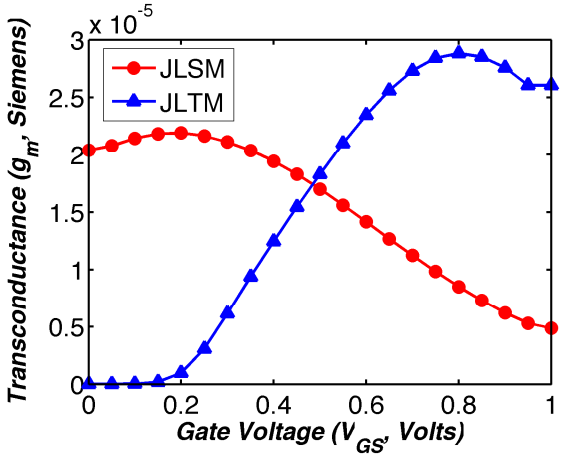

Figure-5(a)

Transconductance (g_m) **at** $(V_{DS} = 1.0V)$

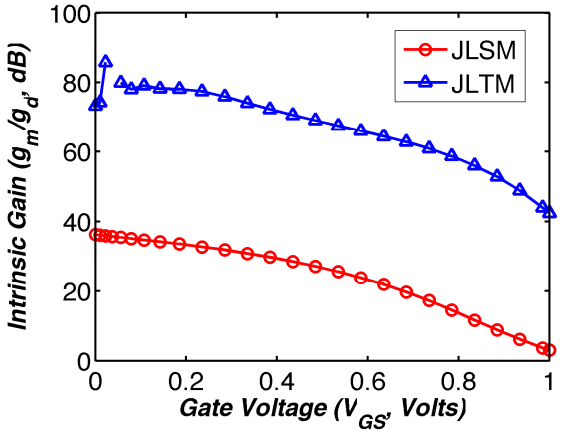

Figure-5(b)

Intrinsic gain $(g_m R_o \, or \, g_m/g_d)$ **at** $(V_{DS} = 1.0V)$

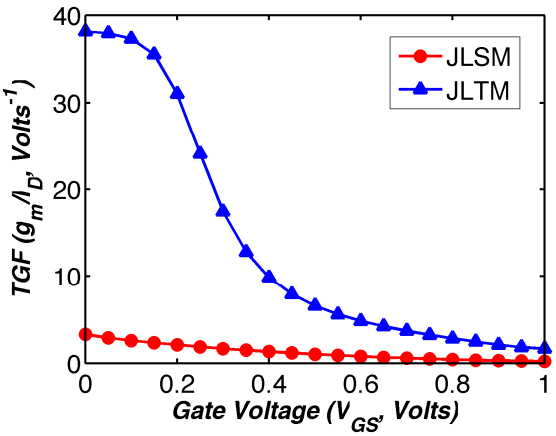

Figure-5(c)

Transconductance generation factor $(TGF, g_m/I_D)$ **at** $(V_{DS} = 1.0V)$

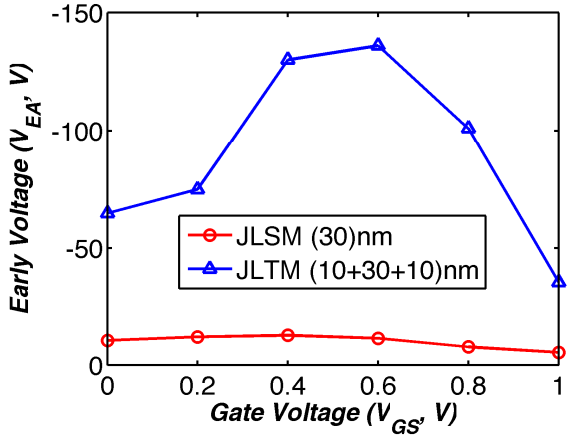

Figure-5(d)

Early voltage (V_{EA}) at $(V_{DS} = 1.0V)$

RF Characteristics: Figure-6 shows the gate capacitance (C_{gg}) and gate-drain capacitance (C_{gd}). Gate capacitance is higher for the JLTM as compared to the JLSM because the total gate area of the former is larger than the latter. Similarly, C_{gd} is also larger for the JLTM. The larger values of capacitance will degrade the ac performance at higher frequencies but since the gain of the JLTM is many times larger than the JLSM, it will compensate to the overall performance of the device.

The other important RF performance parameters are the cutoff frequency (f_T), maximum frequency of oscillation (f_{MAX}) and gain bandwidth product (GBW). The f_T is defined as the frequency at which the short circuit current gain decreases to unity (sometimes referred as the transition frequency), and is given by

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (1)$$

Where g_m is the transconductance and C_{gg} is the gate capacitance.

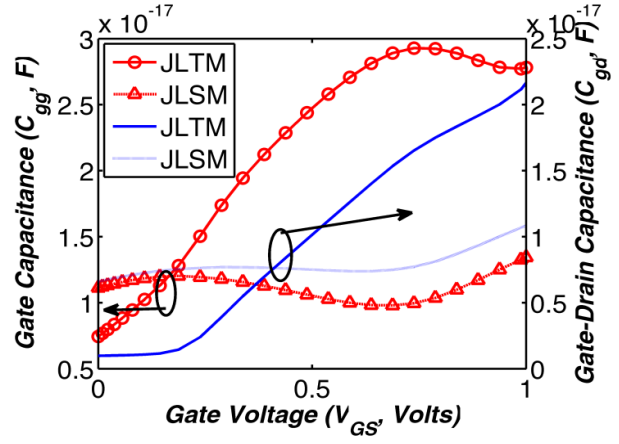

Figure-6

Gate capacitance (C_{gg}) and Gate-Drain capacitance (C_{gd}).

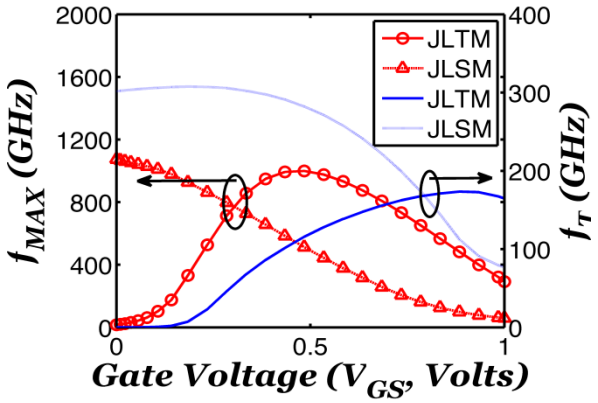

Figure-7(a)

Maximum frequency of oscillation (f_{MAX}) and cutoff frequency (f_T)

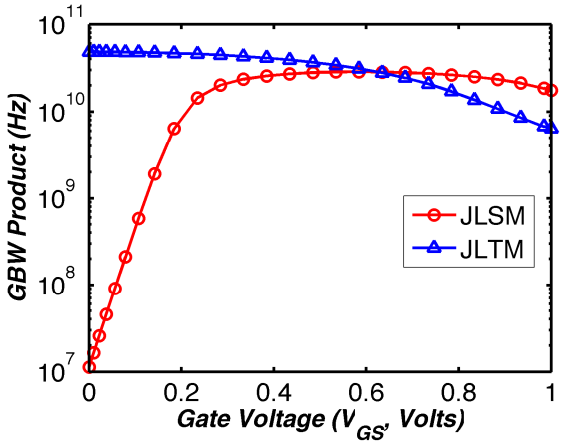

Figure-7(b)

Gain band width (GBW) product

The f_{MAX} is the frequency at which the power gain becomes unity and is given by

$$f_{MAX} = \frac{g_m}{2\pi C_{gs}\sqrt{4\left(g_{ds} + g_m\frac{C_{gd}}{C_{gs}}\right)\left(R_s + R_{ch} + R_g\right)}} \quad (2)$$

Where C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitances respectively, g_{ds} is the output conductance, R_s - source resistance, R_{ch} - channel resistance, and R_g - gate resistance. For the extraction of these parameters ac analysis is performed over a frequency range (here $1\times10^6\ Hz$ to $1\times10^{13}\ Hz$) and Y parameters are computed. After this two port network RF extraction tool (inspect from synopsys sentaurus TCAD) is used to compute the f_T and f_{MAX} using the following equations

$$f_T = f_i \cdot |H_{21}| \quad (3)$$

$$f_{MAX} = f_i \cdot \left[\frac{|Y_{21} - Y_{12}|^2}{4\left[\mathrm{Re}(Y_{11}).\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{21}).\mathrm{Re}(Y_{12})\right]} \right]^{\frac{1}{2}} \quad (4)$$

Where f_i is the input signal frequency.

The f_T and f_{MAX} are compared in figure-7(a). Both parameters are having higher values for JLTM as compared to the JLSM. The GBW is shown for both the MOSFETs in Figure-7(b), which is computed by the following approximate equation

$$GBW = \frac{g_m}{2\pi.10.C_{gd}} \quad (5)$$

The GBW is slightly lower for the JLTM due to larger C_{gd} .

Electrical, DC, Analog and RF Characteristic Variations due to Gate Length Scaling: In this section we discuss the variations of different parameters associated with the JLTM due to length scaling. Figure-8 (a), 8(b), 8(c) and 8(d) shows the variations in the electrostatic potential, electron density, electric field and electron velocity respectively at the SiO_2/Si interface. Electrostatic potential under the gate material $(L1)$ is less affected with the variations in the V_{DS} due to screening effect for the larger gate lengths. Electron density is also relatively higher at the source end for the largest gate length. The electric field along the channel is becoming lower as the gate length is increased, showing a significant reduction in HCEs. Average electron velocity is however, decreased for longer gate lengths.

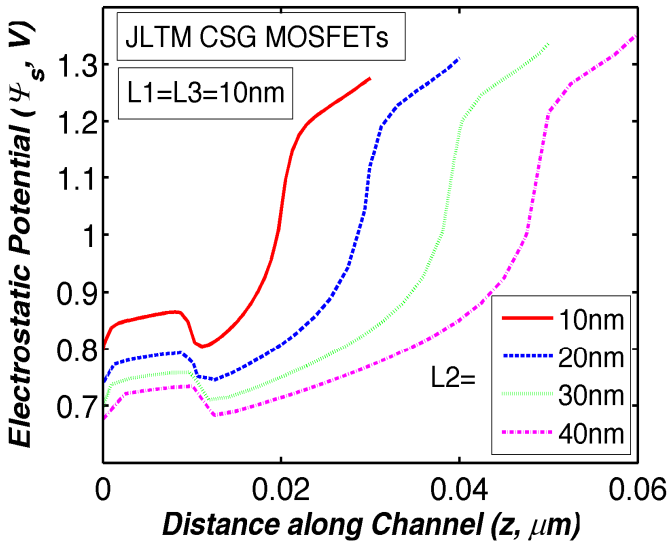

Figure-8(a)

Surface Electrostatic potential (Ψ_s) at $V_{GS} = 1.0V$ and $V_{DS} = 1.0V$

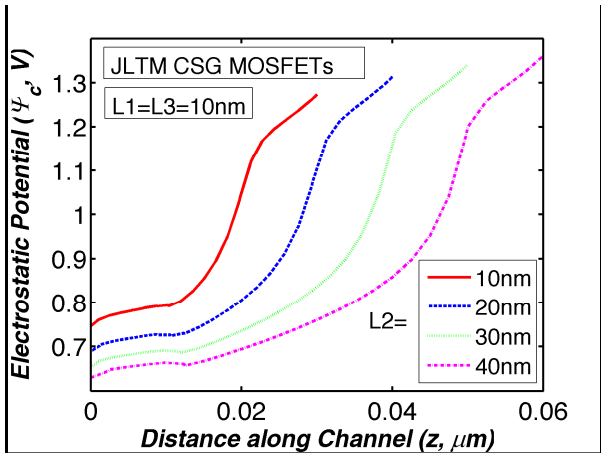

Figure-8(b)

Electrostatic potential in the center of (Ψ_c) at $V_{GS} = 1.0V$ and $V_{DS} = 1.0V$

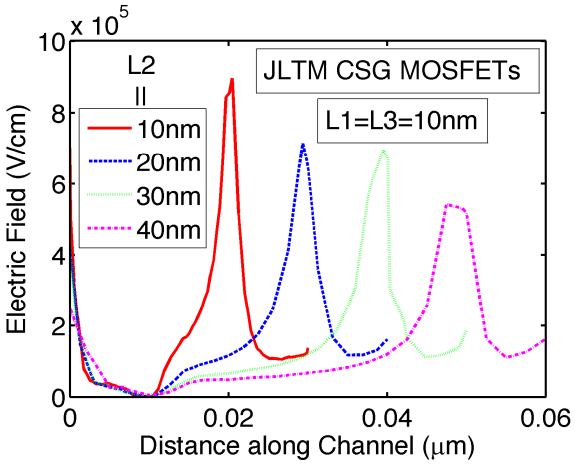

Figure-8(c)

Electric field at $V_{GS} = 1.0V$ and $V_{DS} = 1.0V$

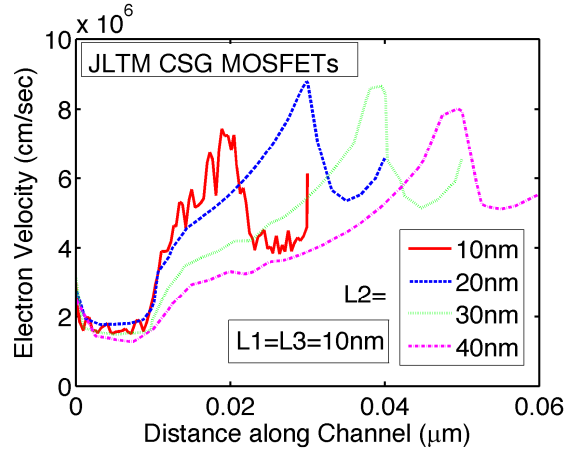

Figure-8(d)

Electron velocity at $V_{GS} = 1.0V$ and $V_{DS} = 1.0V$

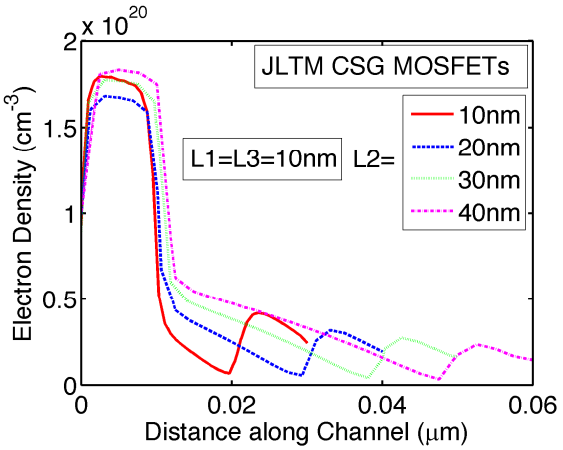

Figure-8(e)

Electron density at $V_{GS}=1.0V$ and $V_{DS}=1.0V$

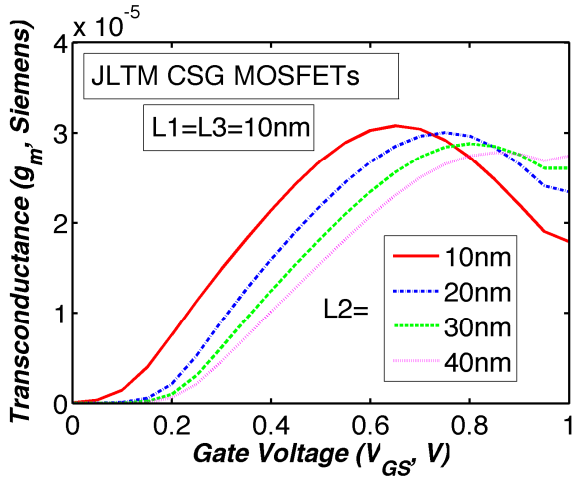

Figure-9(a)

Transconductance (g_m) at $(V_{DS}=1.0V)$

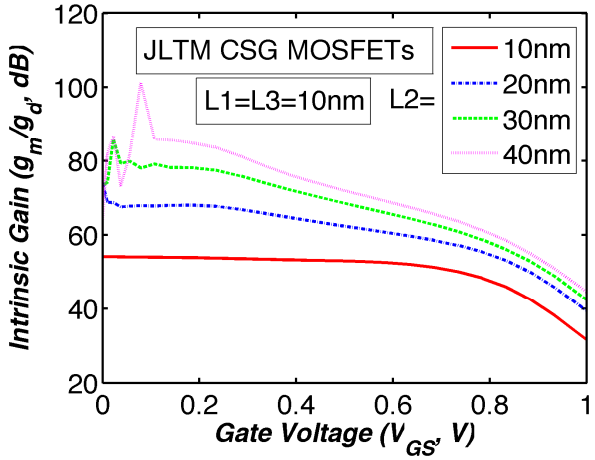

Figure-9(b)

Intrinsic gain $(g_m R_o \text{ or } g_m/g_d)$ at $(V_{DS}=1.0V)$

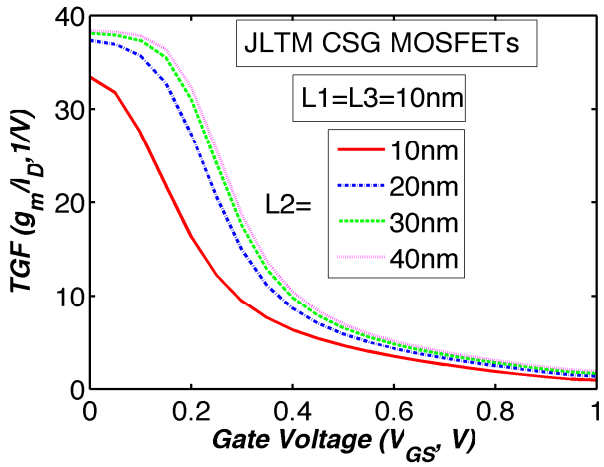

Figure-9(c)

Transconductance generation factor $(TGF, g_m/I_D)$ at $(V_{DS}=1.0V)$

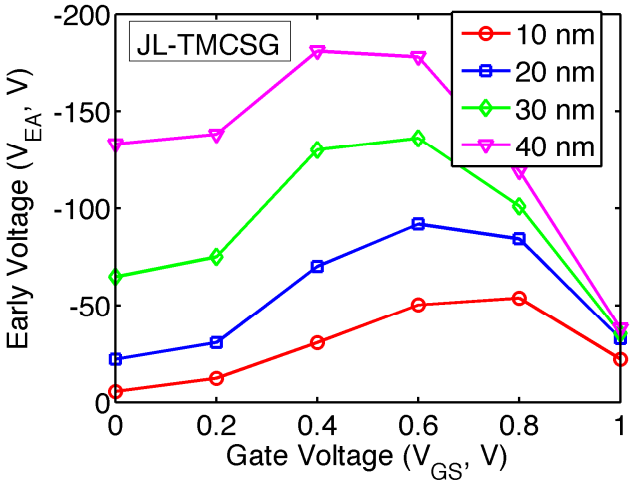

Figure-9(d)

Early voltage (V_{EA}) at $(V_{DS}=1.0V)$

Figure-9(a), 9(b), 9(c) and 9(d) shows the analog behavior scaling of the JLTM with the gate lengths. Transconductance (Figure-9(a)) increases as the gate lengths are scaled down but the intrinsic gain (figure-9(b)) is decreased because of higher output conductance (lower output resistance). The TGF (figure-9(c)) and Early voltage (figure-9(d)) both are scaled down with the gate length. The C_{gg} and C_{gd} variations are shown in the figure-10 (a) and (b) respectively. The C_{gg} is scaled down with the decrease in the gate lengths as expected due to the decrease in the overall gate area, whereas the C_{gd} remains approximately constant (not scaled down).

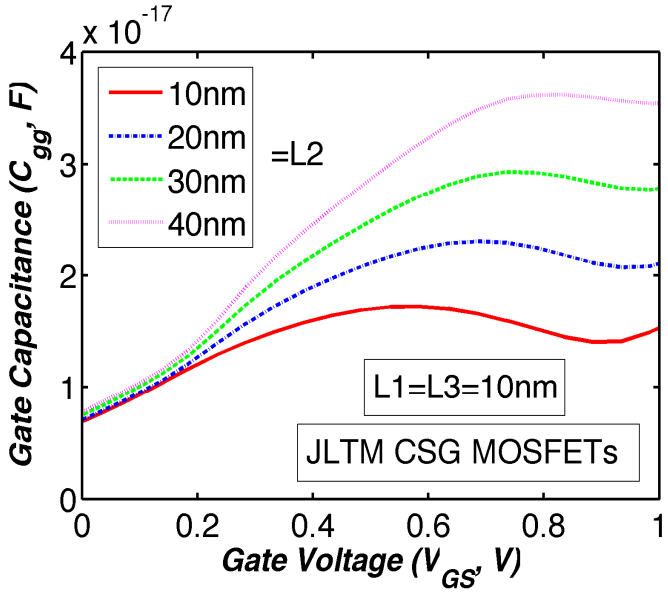

Figure-10(a)
Gate capacitance (C_{gg})

Figure-11(a) and 11(b) compares the scaling of f_T and f_{MAX} respectively. The f_T and f_{MAX} both are higher for the shorter gate lengths due to larger g_m and smaller C_{gg}. Similarly, the GBW product is also higher at the scaled gate lengths as shown in the figure-12.

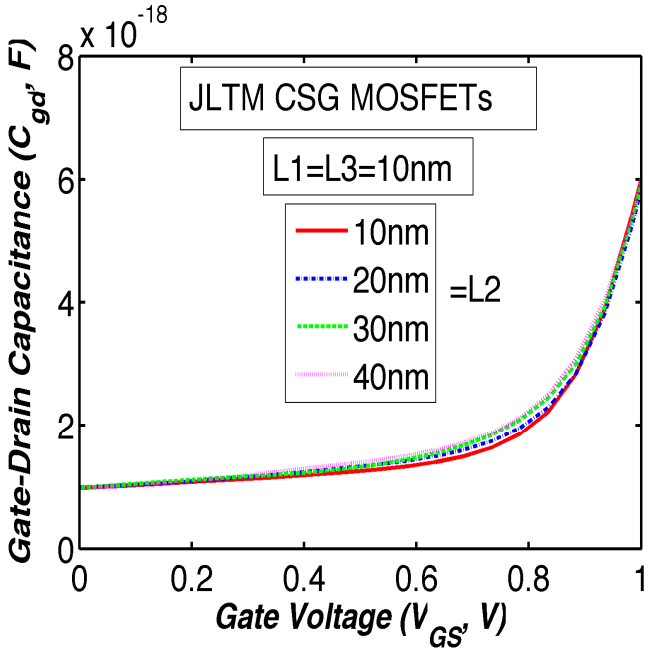

Figure-10(b)
Gate-Drain capacitance (C_{gd})

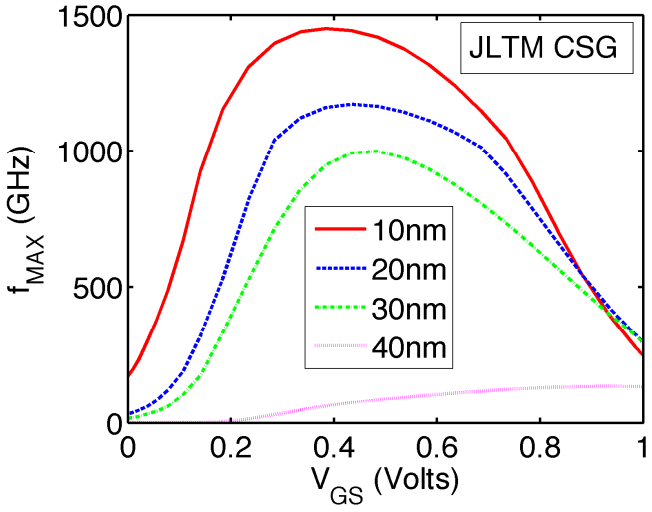

Figure-11(a)
Maximum frequency of oscillation (f_{MAX})

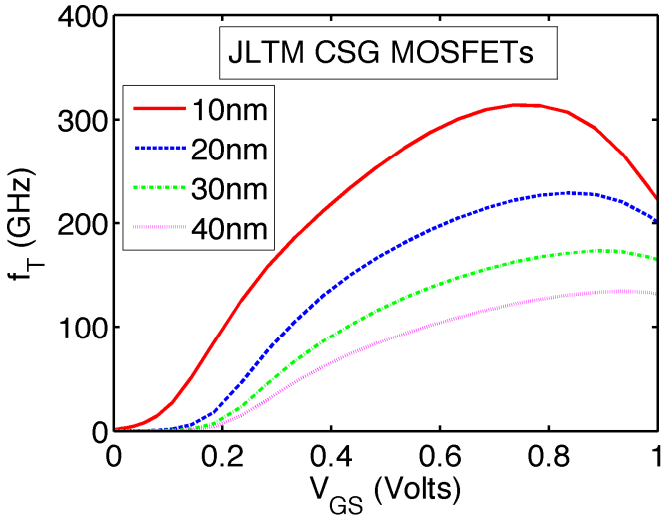

Figure-11(b)
Cutoff frequency (f_T)

Conclusion

The JLTM MOSFETs have been extensively evaluated with the help of 3D TCAD simulation for extracting various DC, analog and RF parameters of importance and compared with that of JLSM. It is observed that the former gives many advantages in terms of higher I_{ON}/I_{OFF} ratio, transconductance g_m, intrinsic gain g_m/g_d, TGF g_m/I_D, Early voltage V_{EA}, cutoff frequency f_T and maximum frequency of oscillation f_{MAX}. Due to these superior qualities of JLTM it may be preferred to be used in digital, analog and RF applications for low power operations. Due to the simplicity of fabrication also (because of non presence of junctions) it looks very attractive to be used at highly scaled gate lengths. A study for the scaling of the

different device parameters with gate length was also carried out. The study reveals that the device parameters are scalable except the C_{gd} .

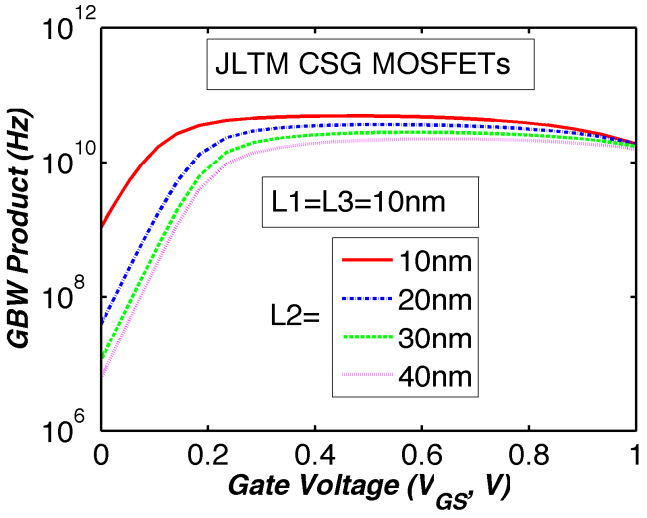

Figure-12
Gain band width (GBW) products

Acknowledgement

This work was supported by the All India Council for Technical Education (AICTE), under Grant 8023/BOR/RID/RPS-253/2008-09 and in part by the grant 21(1)/2005-VCND (Special Manpower Development Program-II Project) of MCIT, DIT (Now DeiTy), Govt. of India.

References

1. Lilienfield, J. E. Method and apparatus for controlling electric current. *US patent*, 1,745,175 **(1925)**

2. Lilienfield, J. E. Device for controlling electric current. *US patent*, 1,900,018 **(1928)**

3. Jean-Pierre Colinge et al, Nanowire transistors without junctions, *Nature Nanotechnology*, **5(3)**, 225 **(2010)**

4. R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn, Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm, *IEEE Electron Device Letters*, **32(9)**, 1170-1172 **(2011)**

5. Suresh Gundapaneni, Swaroop Ganguly, Anil Kottantharayil, Bulk Planar Junctionless Transistor (BPJLT): An Attractive Device Alternative for Scaling, *IEEE Electron Device Letters*, **32(3)**, 261-263 **(2011)**

6. Chun-Jung Su, Tzu-ITsai, Yu-Ling Liou, Zer-Ming Lin, Horng-Chih Lin, Tien-Sheng Chao, Gate-All-Around Junctionless Transistors With Heavily Doped Polysilicon Nanowire Channels, *IEEE Electron Device Letters*, **32(4),** 521-523 **(2011)**

7. Pushpapraj Singh, Navab Singh, Jianmin Miao, Woo-Tae Park, Dim-Lee Kwong, Gate-All-Around Junctionless Nanowire MOSFET With Improved Low-Frequency Noise Behavior, *IEEE Electron Device Letters*, **32(12)**, 1752-1754 **(2011)**

8. Te-Kuang Chiang, A Quasi-Two-Dimensional Threshold Voltage Model for Short-Channel Junctionless Double-Gate MOSFETs, *IEEE Transactions on Electron Devices*, **59(9)**, 2284-2289 **(2012)**

9. Haijun Lou, Lining Zhang, Yunxi Zhu, Xinnan Lin, Shengqi Yang, Jin He, Mansun Chan, A Junctionless Nanowire Transistor with a Dual-Material Gate, *IEEE Transactions on Electron Devices*, **59(7)**, 1829-1836 **(2012)**

10. Gupta Santosh Kumar, Baishya Srimanta, Novel characteristics of Junction less Dual Metal Cylindrical Surround Gate (JLDM CSG) MOSFETs, *Res. J. Recent Sci*, **2(1)**, 44-52 **(2013)**